Quantum gates using a pulsed bias scheme

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We present here a novel scheme to realize quantum gates by means of a pulsed bias. We show how a NOT gate (one qubit), a C-NOT gate (two qubits) and a Toffoli gate (three qubits) can be realized by clocking the bias on one of the qubits in the system. When the bias is kept high, a qubit will remain in the state it has been initialized to, according to the governing two-level Hamiltonian. We call this state a memory state. When the bias is clocked low, the two-level system oscillates between its two basis states. We call this state a transitional state. In all cases, we force one qubit in the system into a transitional state for a certain transitional time. With proper choice of parameters, bias, coupling and tunneling, we show in this talk how these quantum gates can be realized. The key to the C-NOT gate is to maintain the control qubit in a memory state while forcing the target qubit into a transitional state. This reduces the Hamiltonian to a two level system, where the frequency, amplitude, and offset of oscillation of the target qubit are functions of the state of the control qubit. The reduced Hamiltonian approach is then extended further to a Toffoli gate which has two control qubits and one target qubit.