A Directory Based Hybrid Cache Update Strategy to Reduce Memory Latency of Shared Memory Multiprocessors

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Multiple cores with a shared memory on a single-chip provide an excellent architecture to achieve fast computation. However, shared memory multiprocessors with typical write update and write invalidate strategies suffer due to the fact that the number of cores is normally less than 16, bandwidth is often wasted, and memory latency becomes very high. This paper presents a directory based hybrid cache update strategy for shared memory multiprocessors with large number of cores to help reduce memory latency. The proposed directory scheme continuously checks for requests from cores, satisfies the requests according to the priority, starving cases, and updates the directory accordingly. We simulate a 32-core system using pure write update (PWU), pure write invalidates (PWI), and the proposed hybrid strategies. Preliminary experimental results show that the proposed strategy decreases memory latency by 24% when compared with the PWI strategy. The proposed strategy is as good as the PWU strategy.