A PARALLEL LIGHT-EMITTING DIODE STRING DRIVER WITH HIGH DIMMING RATIO

A Thesis by

Jesse Claassen

Bachelor of Electrical Engineering, Wichita State University, 2010

Submitted to the Department of Electrical Engineering and Computer Science
and the faculty of the Graduate School of
Wichita State University
in partial fulfillment of
the requirements for the degree of
Master of Science

May 2015

© Copyright 2015 by Jesse Claassen
All Rights Reserved

A PARALLEL LIGHT-EMITTING DIODE STRING DRIVER
WITH HIGH DIMMING RATIO

The following faculty members have examined the final copy of this thesis for form and content, and recommend that it be accepted in partial fulfillment of the requirement for the degree of Master of Science with a major in Electrical Engineering.

_____
John M. Watkins, Committee Chair

_____
M. Edwin Sawan, Committee Member

_____
Brian Driessen, Committee Member

DEDICATION

To my fiancée, Chelsey,
and my family for their continued support.

ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisor, Dr. Edwin Sawan, for his assistance, guidance, and passion for teaching, which is nothing short of inspirational. I would also like to thank Dr. John Watkins and Dr. Brian Driessen for taking the time to provide feedback on this thesis. I am also particularly thankful for both my parents, who were my first teachers.

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES (continued)

Figure Page

LIST OF FIGURES (continued)

Figure Page

LIST OF ABBREVIATIONS / NOMENCLATURE

ADC	Analog to Digital Converter
CCFL	Cold Cathode Florescent Lamp
CCR	Constant Current Reduction
DAC	Digital to Analog Converter
DC	Direct Current
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
RC	Resistor/Capacitor

ABSTRACT

Light-emitting diodes (LEDs) have become a good alternative to traditional cold cathode fluorescent lamps (CCFLs) for backlighting sources in liquid crystal displays (LCDs). LED backlighting provides a number of benefits over CCFLs, such as greater efficiency, better brightness, longer lifetime, higher dimming ratios, and lower drive circuitry voltage [1]. One application where a higher dimming ratio is desired is in aerospace cockpit LCD modules, which need to provide both high brightness for sunlight readability and also a high dimming ratio for very low brightness during nighttime operation. Two methods commonly used to dim LEDs are constant current reduction(CCR) and pulse width modulation(PWM) dimming. The downside to using CCR is the limited dimming ratio and nonlinearities in light output that occur from variations in luminous efficacy over the dimming range [2]. To obtain a high dimming ratio using PWM dimming, the LED current rise time must be sufficiently faster than the minimum PWM. This ensures that there will be no nonlinearities in the light output, which could result in visible flicker when operating at low-brightness settings. To provide higher system efficiency, a method for soft starting the LED regulator is presented. This method allows for reduced head room operation by ramping the LED current during turn-on, which results in a reduced voltage dip on the LED power supply. Finally, a method for head room adjustment that allows for adjustment of the LED supply voltage for variations in forward voltage over temperature and time is presented.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Due to a number of benefits, light-emitting diodes (LEDs) have become very common in liquid crystal display (LCD) backlighting schemes. Because of the exponential current-voltage relationship of diodes, relatively low forward voltage drop, and search for higher efficiency, it has become common to drive a number of LEDs in series[3]-[7]. Since the light output of LEDs is proportional to the forward current, driving LEDs in series ensures an equal current through each of them. This results in good uniformity and very similar light output from each LED. To provide high pulse width modulation (PWM) dimming ratios, fast LED forward current rise times are required to provide a linear dimming response. This requires consideration of the frequency response of both the LED current regulator along with the power converter supplying power to the LED string. Relatively little research has been done on analysis and design tradeoffs for high-dimming LED string drivers. Most consumer applications do not require high dimming ratios, and as a result, the majority of LED driver-integrated circuits on the market have low dimming ratios below that of 3000:1 [8]-[9], whereas aviation displays can require dimming ratios of up to 10000:1. While a few integrated circuits have been proposed with high dimming ratios [6]-[7], another problem that arises is with component obsolescence. While most consumer electronics are only supported for a few years, aviation electronics are generally required to be supported for much longer lifetimes [10]. With very few high-dimming LED driver options on the market, it can be very difficult to find a replacement if a current component goes to its end of life. To combat this problem, a system could be built using common integrated

circuit components that are readily available on the market and easily replaceable if component obsolescence arises.

1.2 Overview

Chapter 2 provides theoretical background on LED lighting using PWM and constant current regulator (CCR) dimming methods along with gain, lead, and lag loop compensation theory.

Chapter 3 analyzes different current regulator compensation techniques for providing a fast current rise time, which enables high dimming ratios. Section 3.1 provides an overview of the current regulator topology. Section 3.2 provides the operational amplifier model used for analyzing the current regulator. Section 3.3 discusses the common collector amplifier model that is used within the current regulator. Section 3.4 provides the current regulator system model and transfer function. Section 3.5 analyzes gain, lead, and lag compensation techniques to determine the best-suited compensation scheme to yield fast current rise times.

Chapter 4 introduces a soft-start topology, which reduces the output voltage dip when LEDs are initially turned on due to the finite bandwidth of the regulator. Section 4.1 provides an overview of the soft-start topology. Section 4.2 analyzes characteristics of the soft-start turn-on and period. Section 4.3 provides transient response characteristics of the Texas Instruments TPS43060 power supply via simulation using TINA-TI SPICE software. Section 4.4 analyzes efficiency considerations for the soft-start topology for both power dissipation and overall system efficiency gains.

Chapter 5 introduces a topology for head room adjustment that allows for minimizing power dissipated in the pass transistor of the current regulator. Section 5.1 provides an overview of the head room adjustment topology. Section 5.2 demonstrates how the analog-to-digital

converter (ADC) measurements can be made at the collector of the current regulator. Section 5.3 analyzes an output voltage adjustment circuit and provides component value selection for implementation.

Chapter 6 concludes this work and summarizes the results.

CHAPTER 2

THEORETICAL BACKGROUND

2.1 Introduction

This chapter provides the theoretical background for feedback stability, compensation techniques, and LED dimming methods.

2.2 Feedback Stability

2.2.1 Feedback

The feedback stability analysis performed in this thesis was done by analyzing the poles and zeros of a given transfer function. The feedback system is demonstrated in Figure 1.

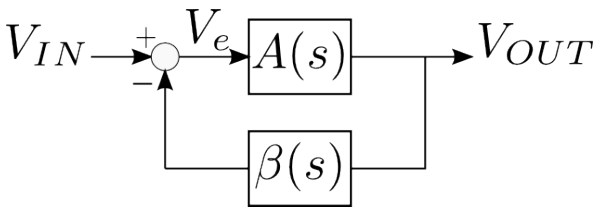

Figure 1. Feedback system.

where

$$V_{OUT} = V_e \cdot A(s) \tag{1}$$

$$V_e = V_{IN} - V_{OUT} \cdot \beta(s) \tag{2}$$

Solving for the transfer function yields

$$\frac{V_{OUT}}{V_{IN}} = \frac{A(s)}{1 + A(s) \cdot \beta(s)} \tag{3}$$

The poles of the system can be found by setting the characteristic equation to zero:

$$1 + A(s) \cdot \beta(s) = 0 \tag{4}$$

As shown in equation (4), varying the feedback factor β affects the poles of the system transfer function.This feedback effect on the poles is dependent on the order of the system.

2.2.2 Loop Gain

Loop gain is the product of the transfer functions in the forward and feedback loops. From Figure 1, the loop gain is given by

$$Loop\ Gain = A(s) \cdot \beta(s) \tag{5}$$

The loop gain can be used to analyze the stability of the system. In equation (5), it is assumed that both the plant $A(s)$ and feedback factor $\beta(s)$ are functions of frequency. The loop gain can be expressed in complex terms as

$$|A(s) \cdot \beta(s)| \angle \theta(\omega) \tag{6}$$

At the frequency where $\theta(\omega) = 180°$, the feedback is no longer negative but rather positive. When this occurs, the magnitude of the loop gain can be one of the following:

$$Case\ 1: |A(s) \cdot \beta(s)| < 1 \tag{7}$$

$$Case\ 2: |A(s) \cdot \beta(s)| = 1 \tag{8}$$

$$Case\ 3: |A(s) \cdot \beta(s)| > 1 \tag{9}$$

For case 1, it can be seen from equation (4) that system poles will still reside in the left-half plane, and the system is stable. The transient response will decay according to the real component of the system poles. For case 2, poles reside on the imaginary axis, and the system will be marginally stable. Here, the transient portion of the response does not decay, and sustained oscillations will occur. For case 3, poles will reside in the right-half plane, and the system will be unstable. The transient portion of the response will grow until bounded by system limitations.

2.2.3 Phase and Gain Margin

Phase margin provides a measure of the system's stability and is determined from a bode plot of the loop gain, $A(s) \cdot \beta(s)$:

$$Phase\ Margin = \theta(\omega) + 180° \tag{10}$$

where frequency ω, (at which point $|A(s) \cdot \beta(s)| = 1$) is the frequency used to evaluate the system phase shift $\theta(\omega)$. If the $phase\ margin < 0°$, then the system will be unstable. The gain margin is the difference in magnitude between $|A(s) \cdot \beta(s)|$ at $\theta(\omega) = -180°$ and unity gain crossover. This value is generally expressed in decibels (dB). If $|A(s) \cdot \beta(s)| > 0dB$ at $\theta(\omega) = -180°$, then the system will be unstable. Figure 2 demonstrates graphically the gain and phase margins.

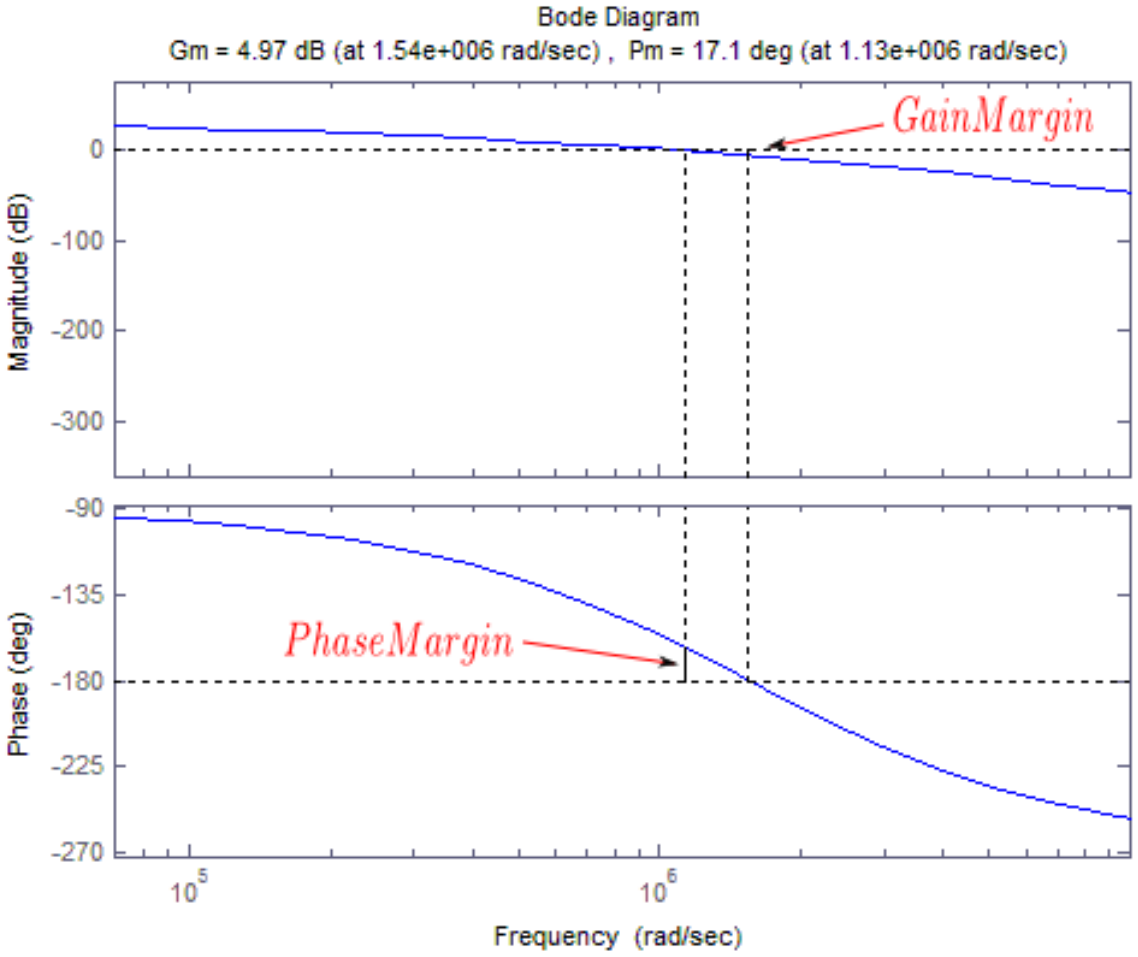

Figure 2. Representation of gain and phase margins.

2.3 Compensation Techniques

2.3.1 Gain Compensation

Gain compensation is achieved by reducing the loop gain of the system. This can be performed in either the forward loop or feedback loop. Gain compensation works by reducing the crossover frequency of the system, and as a result, the gain and phase margins are increased. The main drawback to this compensation method is the reduced crossover frequency. Figure 3 shows the reduced crossover frequency from the reduced loop gain.

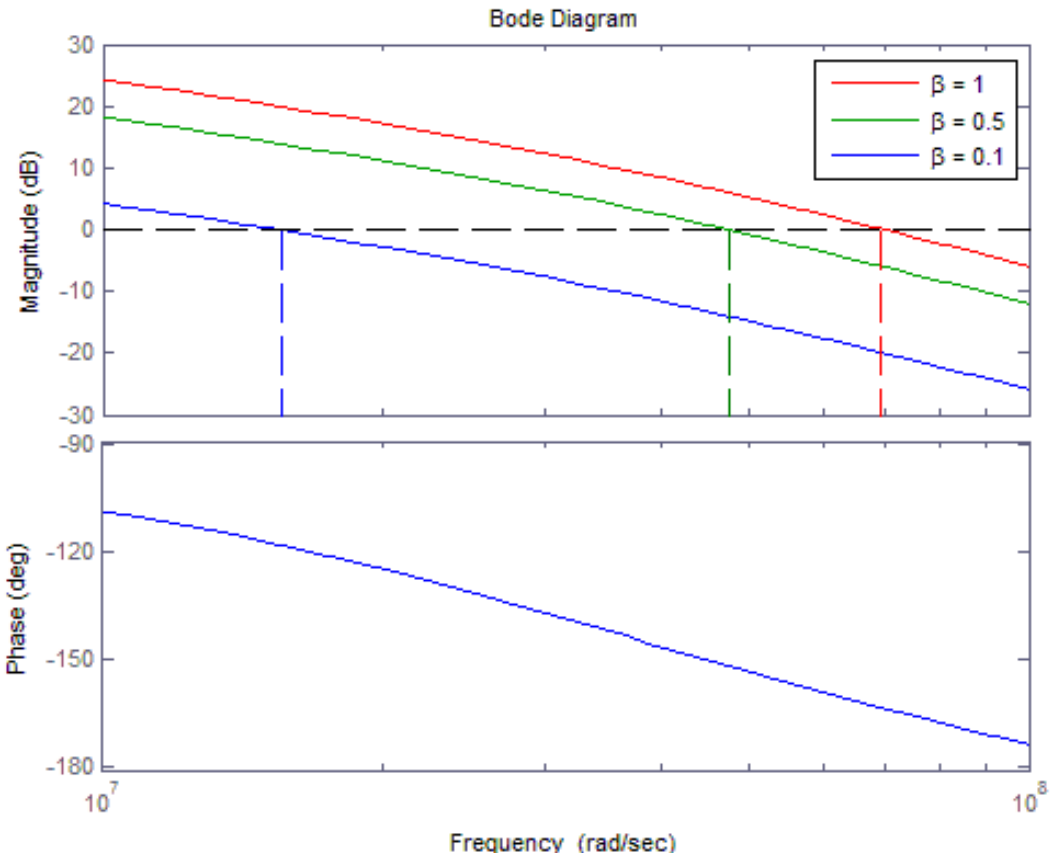

Figure 3. Gain compensation example.

2.3.2 Lead Compensation

Lead compensation networks are used to provide a positive phase shift. The lead compensation network utilized in this thesis contains a lower frequency zero and a resulting

higher frequency pole. A lead compensation network can be used to extend the crossover frequency of the system. This is accomplished by placing the lead zero near the crossover frequency. The resulting pole is placed beyond the crossover frequency so that an additional phase lag does not contribute to instabilities. Figure 4 shows a bode diagram of a lead network.

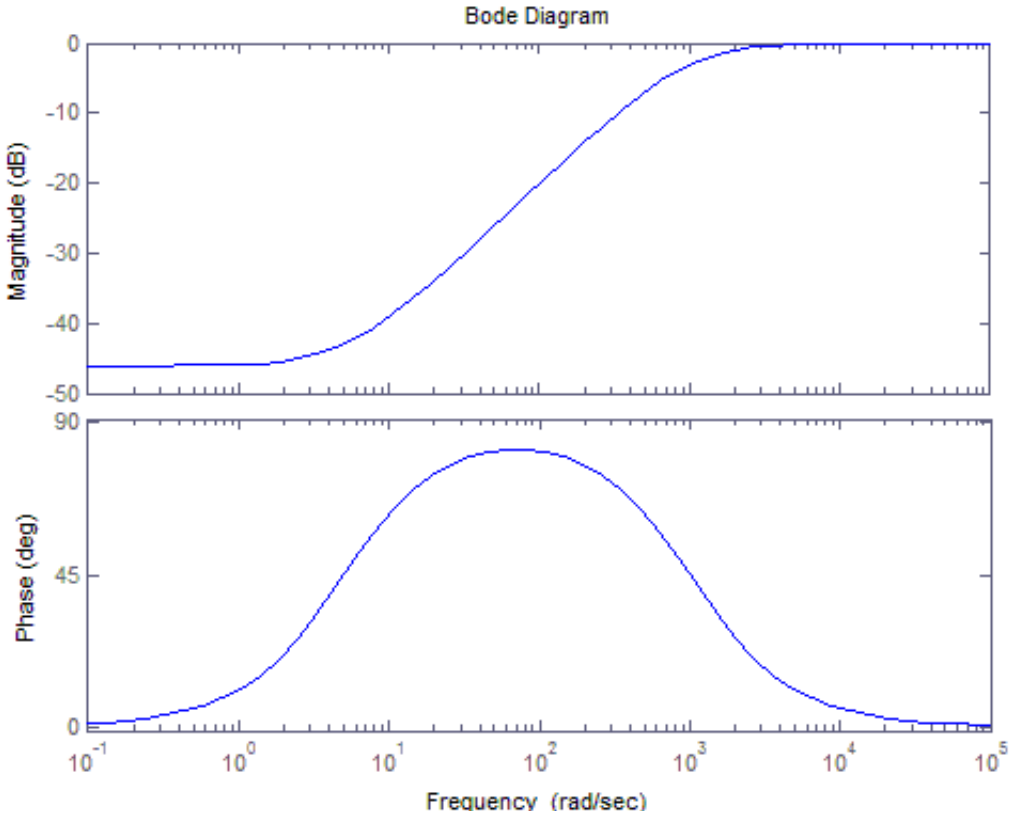

Figure 4. Lead compensation network.

2.3.3 Lag Compensation

Lag compensation is used to reduce the loop gain so that crossover occurs at a lower frequency. This is done by adding a pole and zero into the transfer function. The pole is used to increase loop gain roll-off prior to crossover. The zero is placed prior to crossover to provide a positive phase shift in order to remove the negative phase shift contributed by the lag pole. A bode diagram of a lag network is shown in Figure 5.

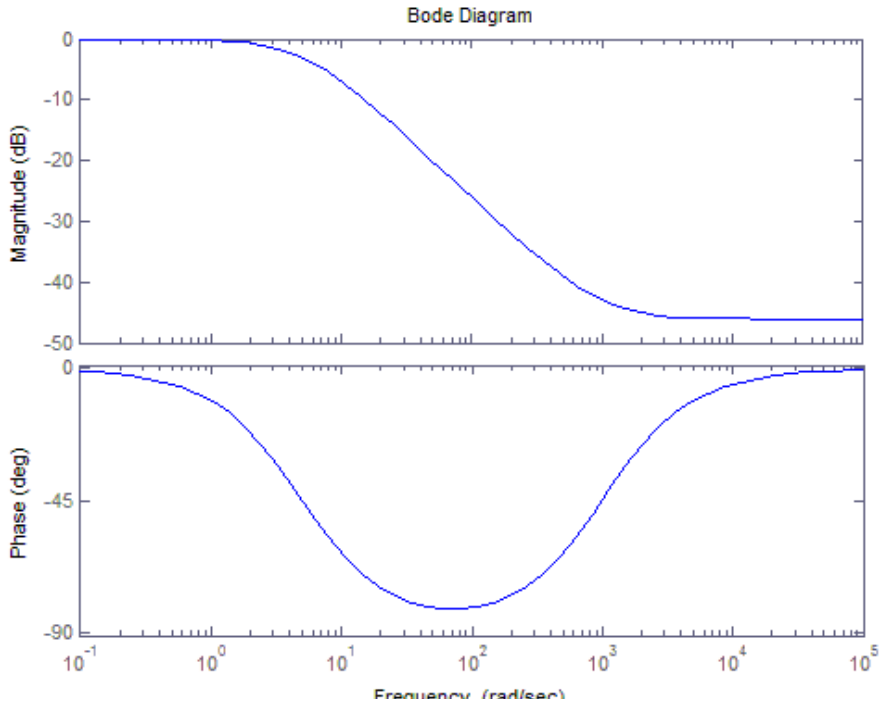

Figure 5. Lag compensation network.

2.4 LED Dimming Methods

2.4.1 Pulse Width Modulation Dimming

Pulse width modulation dimming is performed by varying the duty cycle of the LED current waveform, where by the average LED current can be used for dimming. PWM switching is performed at a higher frequency than the human eye can perceive; thus, the average LED current rather than the switching of LEDs from full brightness to zero brightness is perceived. PWM dimming is shown in Figure 6.

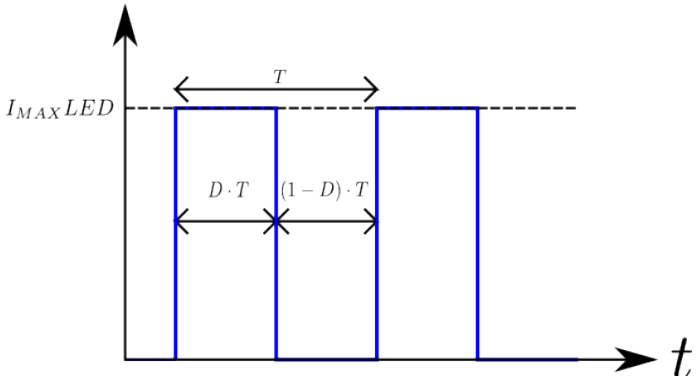

Figure 6. PWM dimming at 50% duty cycle.

The average LED current is given by

$$I_{LED\_AVG} = D \cdot I_{MAX}LED \tag{11}$$

where $I_{MAX}LED$ is the recommended LED current, which is provided in the manufactures datasheet.

2.4.2 Constant Current Reduction Dimming

Constant current reduction dimming, as shown in Figure 7, is performed by varying the direct current (DC) that flows through the LED. Its magnitude can be varied to obtain the desired brightness up to the maximum specified LED current given in the manufacturer's datasheet.

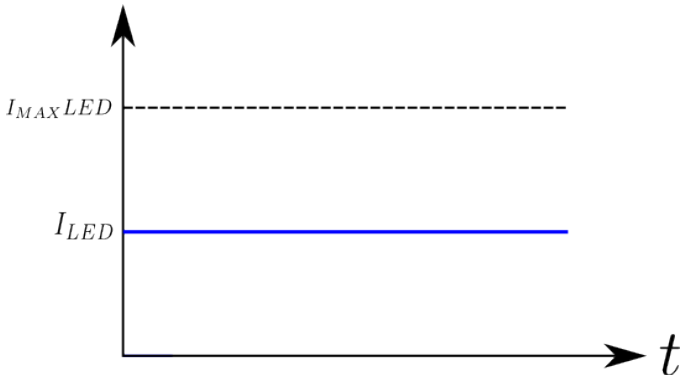

Figure 7. CCR dimming at 50% rated LED current.

One downside to using CCR dimming is that datasheet specifications are no longer valid when the magnitude in the current is varied from the datasheet specification. Potential shifts in forward voltage, chromaticity, and efficacy of the LED may occur when operating the LED outside datasheet specifications.

2.4.3 Efficacy Shifts in CCR vs. PWM Dimming

Luminous efficacy of an LED is the ratio of luminous flux to the electrical power supplied to the LED. It is a measure of how well the LED produces light in the visible spectrum

of the human eye. Previous research work has shown that large changes in efficacy can occur when using CCR dimming [13], as shown in Figure 8.

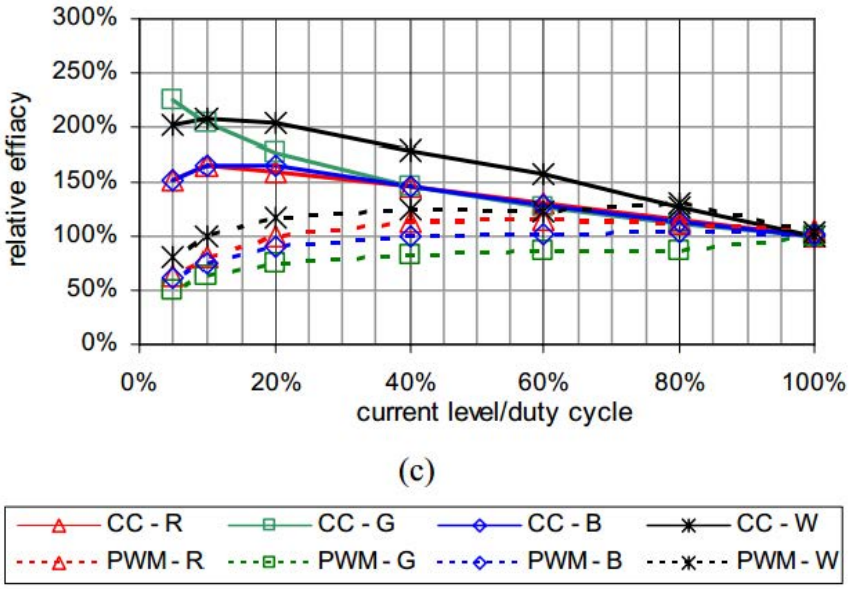

Figure 8. Efficacy shifts of PWM vs. CCR for red, green, blue, and white LEDs (reprinted from [2], SPIE).

The large shifts in efficacy for CCR dimming are undesired due to the non-linearity that is added to the LED current vs. light output curve.

CHAPTER 3

CURRENT REGULATOR

3.1 Current Regulator Overview

The current regulator is composed of an operational amplifier, pass transistor and current sense resistor. Its objective is to vary the impedance of the pass transistor to maintain a defined current through the transistor. The current regulator is used to provide a consistent forward current through the LED string and is required due to the exponential forward I-V relationship of LEDs. Figure 9 demonstrates the implementation of a current regulator.

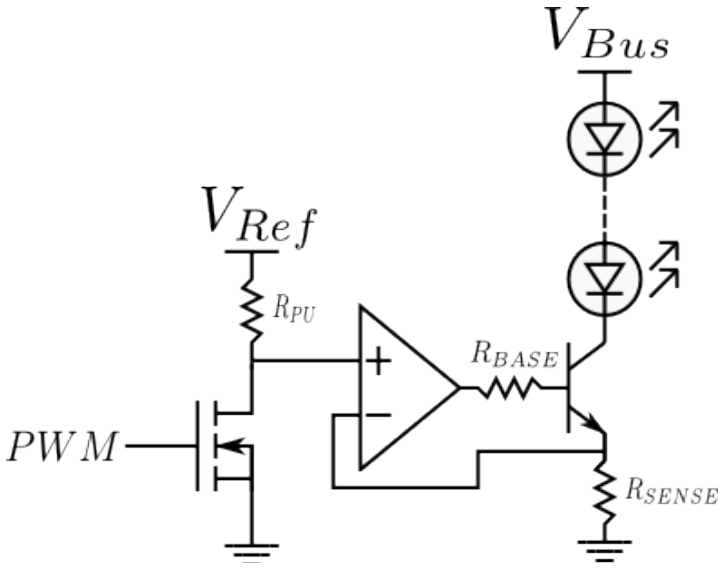

Figure 9. Current regulator for LED string.

The current regulator maintains the LED string current to a value determined by V_{REF} and R_{SENSE}, and is given by

$$I_{LED} = \frac{V_{REF}}{R_{SENSE}} \tag{12}$$

The current regulator provides dimming by applying a PWM signal to a metal oxide semiconductor field effect transistor (MOSFET) connected to the non-inverting pin of the

operational amplifier. When the PWM signal is applied, the non-inverting pin of the operational amplifier is pulled to the ground, and the LED string current is reduced to zero. When the PWM signal is removed, the non-inverting pin of the operational amplifier is pulled up to V_{REF}, and the LED current is increased to the value given by equation (12). To provide high dimming ratios using PWM dimming, the rise and fall times of the LED current must be fast. For this design, a 10,000:1 dimming ratio at 120Hz is the objective. At the minimum dimming signal, the current pulse width is defined by

$$Minimum\ Current\ Pulse\ Width\ = \frac{1/_{120\ Hz}}{10{,}000} \approx 833ns \tag{13}$$

For PWM dimming to provide a linear light vs. duty cycle output curve, the rise and fall times of the LED current must be much smaller than the pulse width. A design objective of rise and fall times less than 1/10th of the minimum pulse width is defined. This results in desired rise and fall times less than approximately 83ns.

3.2 Operational Amplifier Model

The operational amplifier is modeled by a two-pole transfer function, which is representative of many commercial operational amplifiers. This model consists of a dominant pole at low frequency and a high-frequency pole located at the 0dB crossover frequency of the amplifier. This implies that at the 0dB crossover frequency, the low-frequency pole contributes $-90°$ of phase shift, while the high-frequency pole contributes another $-45°$ of phase shift. Thus, $-135°$ of phase shift is accumulated in the loop, and a $45°$ phase margin exists. The approximate locations of the low-frequency pole, high-frequency pole, and crossover frequency can be found in the manufacturer's datasheet.

The transfer function of the operational amplifier is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_{OL}}{\left(\frac{1}{2\pi \cdot Low\ Pole} \cdot s + 1\right)\left(\frac{1}{2\pi \cdot High\ Pole} \cdot s + 1\right)} \tag{14}$$

whereA_{OL} is the DC open-loop gain of the amplifier. An approximation of this value is given in the manufacturer's datasheet. This value can also be approximated by using the high- and low-frequency pole values. The approximation is made by observing that at low frequencies, prior to the first pole, the gain is flat. After the first pole, the gain decreases at a rate of –20dB per decade in frequency until the second pole, which is located at 0dB, or a gain of 1. This implies that the total gain roll-off is given by

$$Total\ Gain\ Roll\ Off\ (dB) = 20 \cdot \log\left(\frac{High\ Pole}{Low\ Pole}\right) \tag{15}$$

which shows that the approximate value of A_{OL}in the transfer function is simply the ratio of the high-frequency pole to the low-frequency pole:

$$A_{OL} = \frac{High\ Pole}{Low\ Pole} \tag{16}$$

The amplifier used for system modeling and simulation has the following characteristics:

$$High\ Pole = 80MHz \tag{17}$$

$$Low\ Pole = 200Hz \tag{18}$$

$$A_{OL} = \frac{80MHz}{200Hz} = 400{,}000 \tag{19}$$

which yields the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = \frac{400{,}000}{(7.96 \cdot 10^{-4} \cdot s + 1)(1.99 \cdot 10^{-9} \cdot s + 1)} \tag{20}$$

The bode plot of equation (20) is shown in Figure 10.

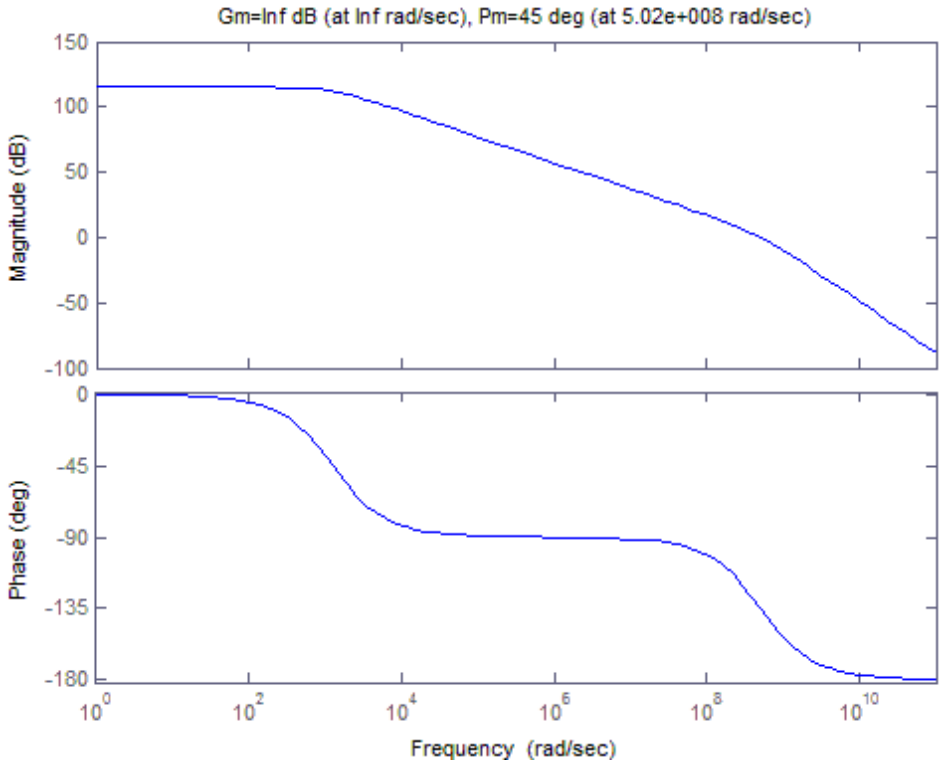

Figure 10. Bode plot of operational amplifier transfer function.

3.3 Common Collector Amplifier Model

The common collector amplifier is modeled with the added base resistorR_{BASE}, and current sense resistor R_{SENSE}. The base-to-emitter resistance is modeled as a small signal input resistance r_π, which is dependent on the transistor gain h_{FE} and the collector current. The collector current is modeled as an independent current source, the value of which is determined by the base current and transistor gain h_{FE}. Since parasitic capacitances associated with the transistor are not generally given in the manufacturer's datasheet, no capacitances are included in the model. A circuit model of the common collector amplifier is provided in Figure 11.

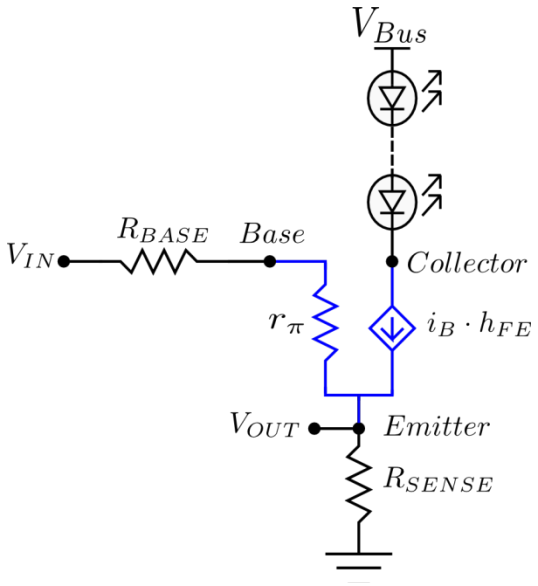

Figure 11. Equivalent circuit for common collector amplifier.

The transition frequency of the transistor is used to model the frequency dependence of the circuit. The transition frequency is the unity gain frequency of the transistor and is generally included in the manufacturer's datasheet. The transition frequency f_T,along with the transistor current gain h_{FE} is are used to determine the –3dB break frequency f_B:

$$f_B = \frac{f_T}{h_{FE}} \tag{21}$$

To determine the transfer function, the V_{IN} and V_{OUT} terminals of the circuit are labeled as shown in Figure 11. Equations (22) and (23) are used to describe the circuit.

$$V_{OUT} = i_B \cdot (1 + h_{FE}) \cdot R_{SENSE} \tag{22}$$

$$i_B = \frac{V_{IN} - V_{OUT}}{R_{BASE} + r_\pi} \tag{23}$$

Combining these equations and simplifying yields

$$\frac{V_{OUT}}{V_{IN}} = \frac{(1 + h_{FE}) \cdot R_{SENSE}}{(1 + h_{FE}) \cdot R_{SENSE} + R_{BASE} + r_\pi} \tag{24}$$

Next, the pole as described by the transition frequency is added to the transfer function to represent the gain attenuation seen at high frequency:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{(1+h_{FE})\cdot R_{SENSE}}{(1+h_{FE})\cdot R_{SENSE}+R_{BASE}+r_\pi}}{\frac{h_{FE}}{2\pi\cdot f_T}\cdot s+1} \tag{25}$$

Note that the break frequency is determined by f_T and h_{FE}, and is reduced as h_{FE} increases.

For this design, the common collector amplifier will have the following properties:

$$h_{FE} = 100 \tag{26}$$

$$R_{SENSE} = 1\Omega \tag{27}$$

$$R_{BASE} = 300\Omega, \qquad r_\pi = \frac{H_{FE}\cdot V_T}{I_C} = 16.6\Omega \tag{28}$$

$$f_T = 500MHz \tag{29}$$

A bode diagram of the common collector amplifier is shown in Figure 12.

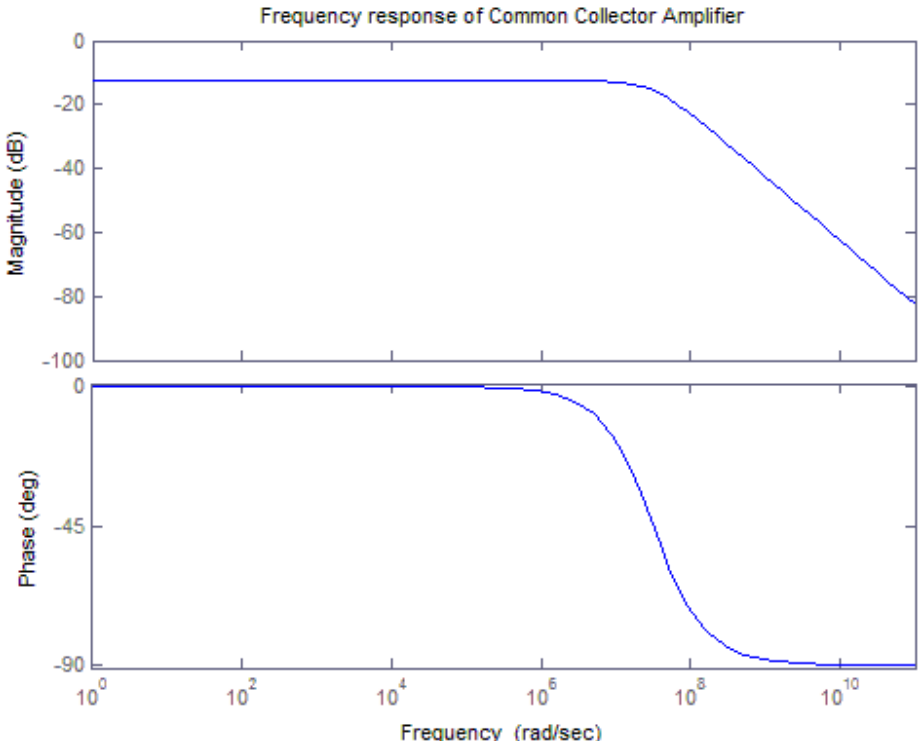

Figure 12. Frequency response of common collector amplifier.

3.4 Current Regulator System Model

The equivalent closed-loop current regulator is shown in Figure 13, and further simplified in Figures 14 and 15.

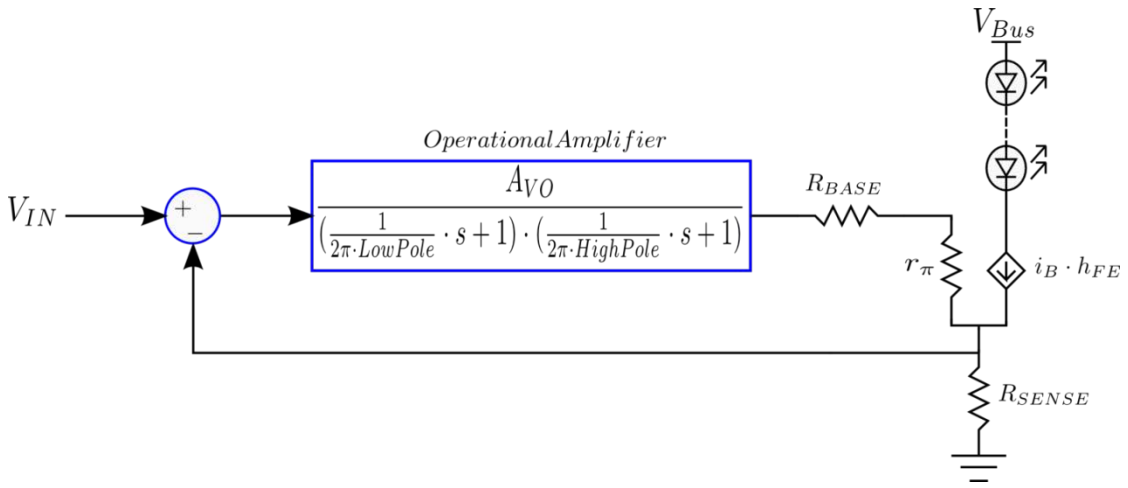

Figure 13. Equivalent closed-loop current regulator circuit.

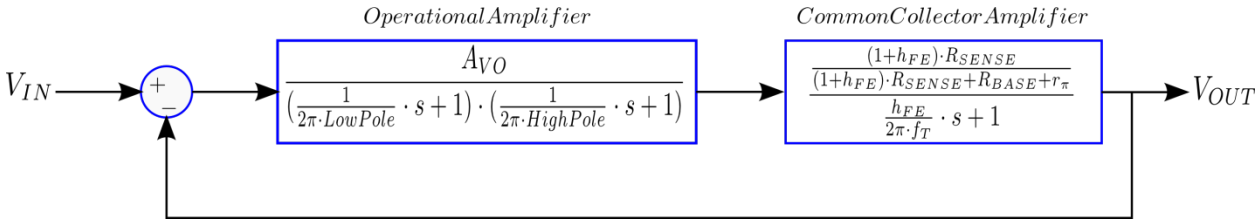

Figure 14. Equivalent closed-loop current regulator system.

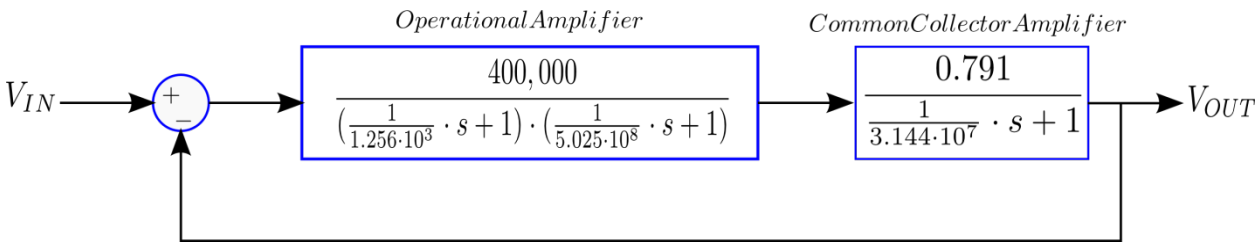

Figure 15. Closed-loop system with substituted design values.

By inspection, it can be seen that the break frequency of the common collector amplifier is below that of the high-frequency pole of the operational amplifier. Given that the operational amplifier is designed for a typical phase margin of 45°, and the addition of a third system pole from the common collector amplifier is in close proximity to the high-frequency operational amplifier pole, a reduction in phase margin and a resulting under-damped step response can be assumed. A bode plot of the current regulator system is shown in Figure 16, and the resulting step response of the system is provided in Figure 17. Figure 16 shows that the phase margin has been reduced to 16.7° due to the addition of the common collector amplifier's pole, and the resulting step response shows an under-damped system response.

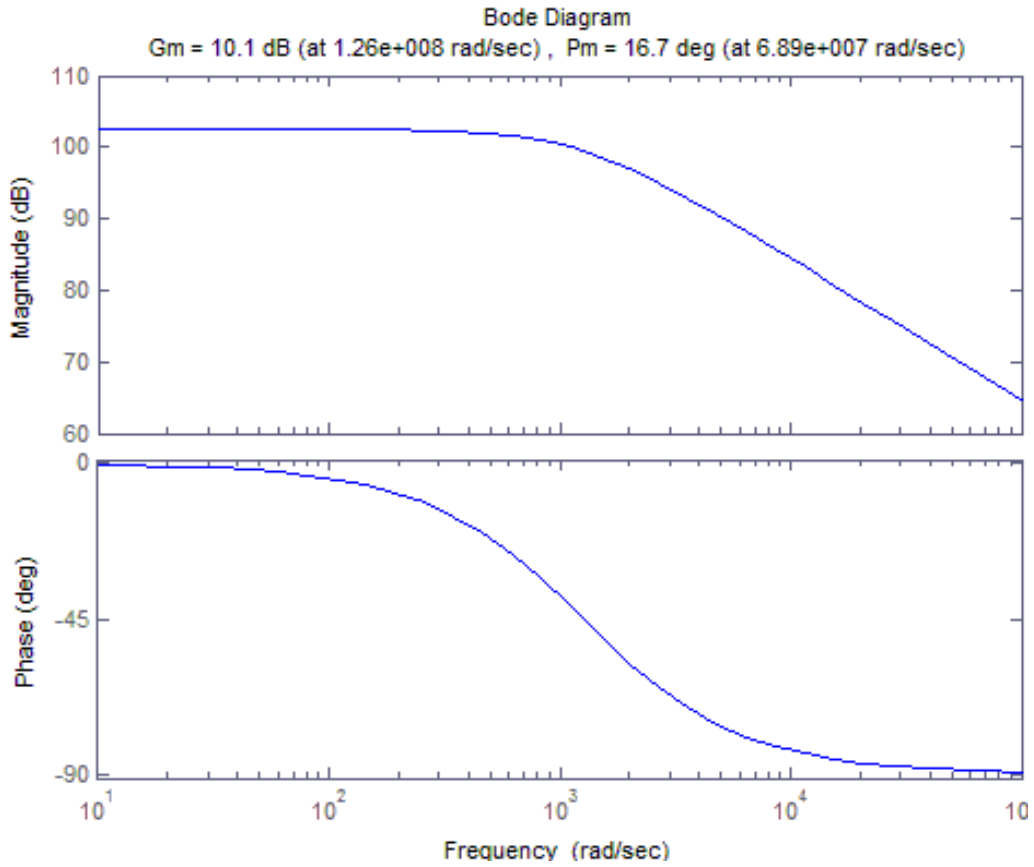

Figure 16. Current regulator loop phase and gain margins.

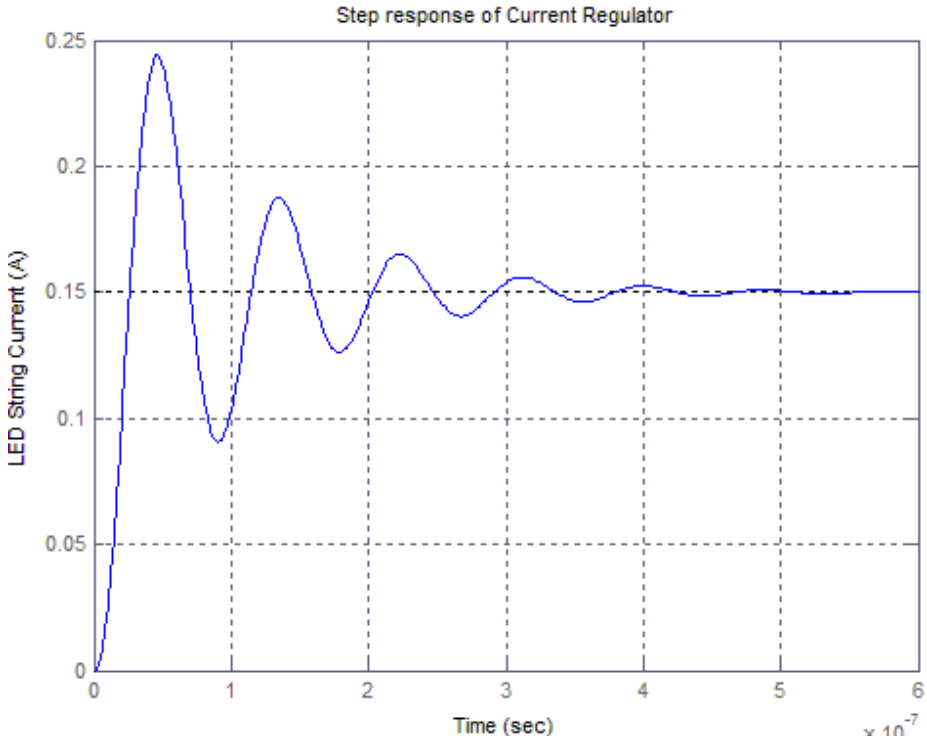

Figure 17. Current regulator step response.

3.5 Current Regulator Compensation

With a resulting phase margin of 16.7°, the step response exhibits an unsatisfactory overshoot and settling time, and must be compensated to ensure stability across temperature and parameter variations. A number of different loop compensation methods will be discussed relative to advantages and tradeoffs.

3.5.1 Gain Compensation

Gain compensation is used to reduce the loop gain, which ultimately reduces the crossover frequency of the system. The reduction in crossover frequency is meant to reduce the amount of accumulated phase lag, which increases the phase margin. For this system, the common collector amplifier has a voltage gain of less than 1 and is heavily influenced by the selection of the base resistance R_{BASE}, as shown in Figure 18.

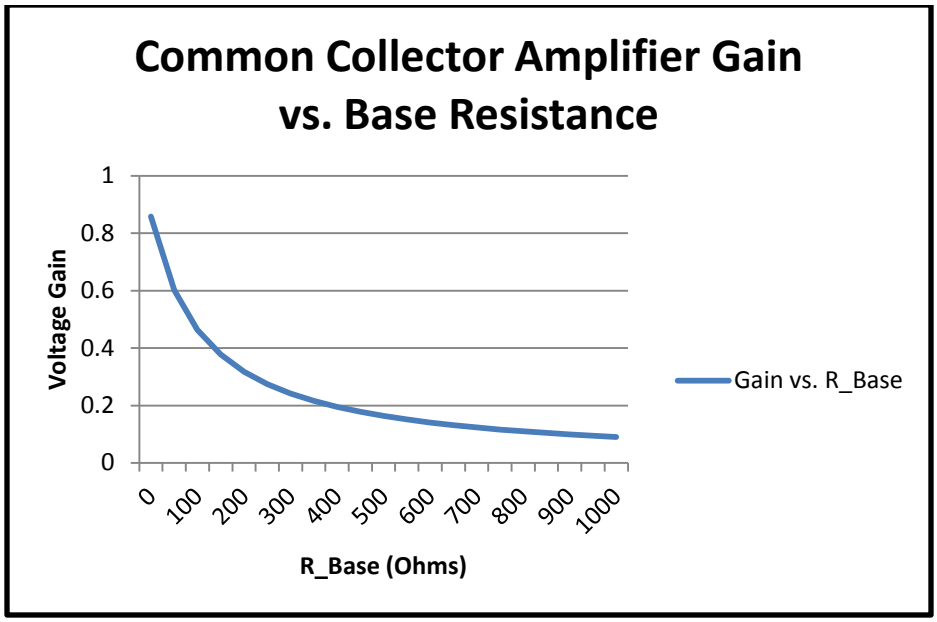

Figure 18. DC gain vs. R_{BASE}.

As the base resistance is increased, the DC voltage gain of the common collector amplifier decreases. Figure 19 plots the loop gains with various base resistance values to demonstrate the reduced crossover as the base resistance is increased.

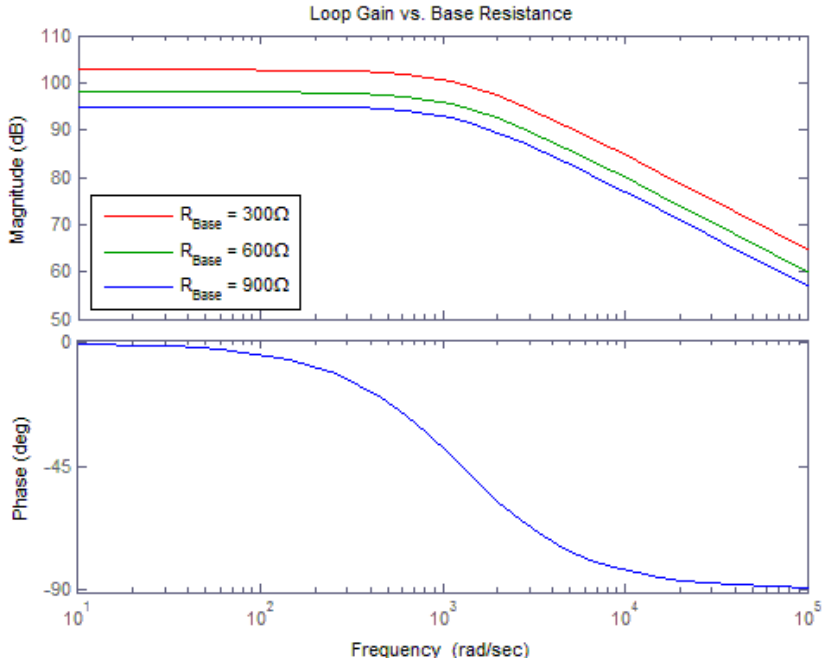

Figure 19. Loop gain vs. base resistance.

Figure 20 plots the step response with various base resistance values. Here, R_{BASE} provides a simple means for gain compensation of the system loop. A second method of gain compensation that can be used is an attenuation network in the feedback loop, which reduces the amount of feedback, as demonstrated in Figure 21.

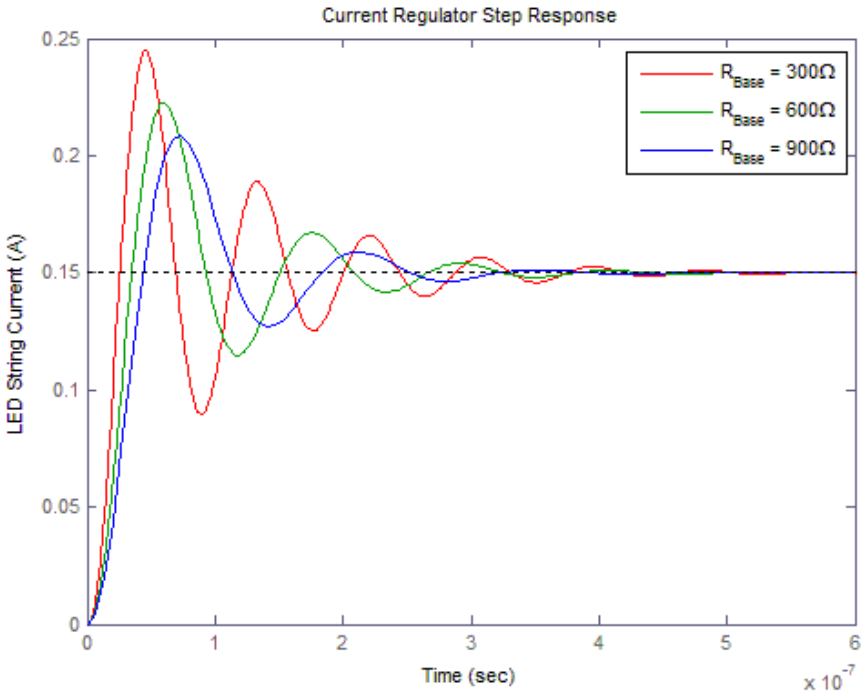

Figure 20. Step response with different base resistance values.

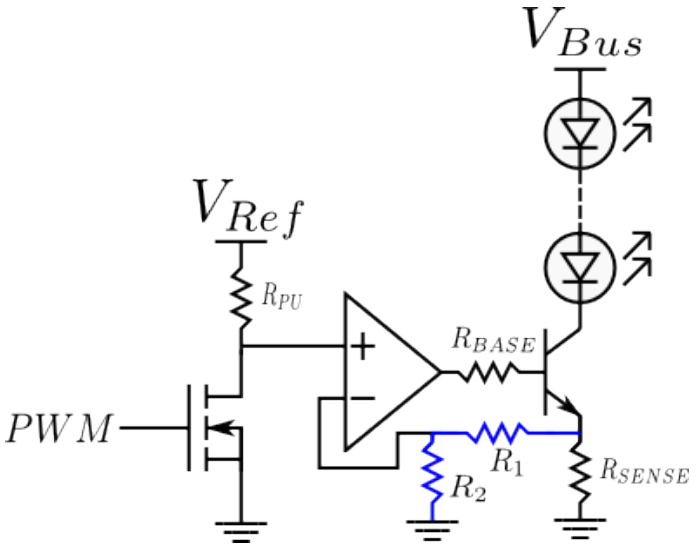

Figure 21. Gain compensation implemented in feedback loop.

Since attenuation is performed in the feedback loop, the input signal must be scaled down by a value that is proportional to the feedback factor β:

$$\beta = \frac{R_2}{R_2 + R_1} \tag{30}$$

$$VIN_{Scaled} = VIN \cdot \beta \tag{31}$$

Scaling input according to the feedback factor will keep the LED string current at the desired magnitude. A bode plot with various amounts of feedback is shown in Figure 22, and the corresponding step responses are shown in Figure 23.This demonstrates that gain compensation can be implemented in either the forward loop or the feedback loop of the system.

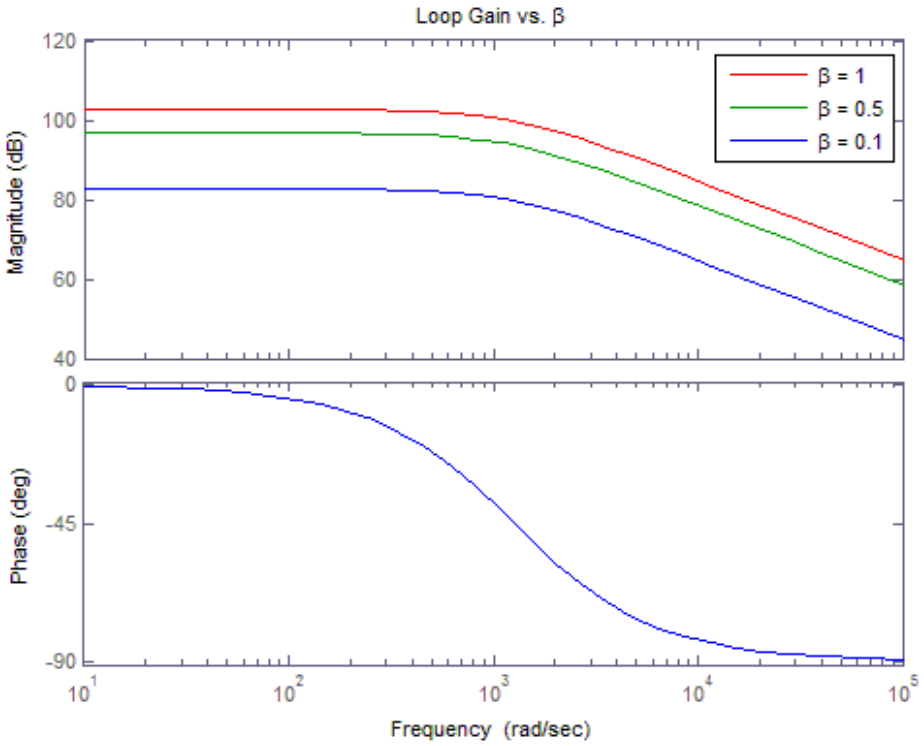

Figure 22. Loop gain vs. β.

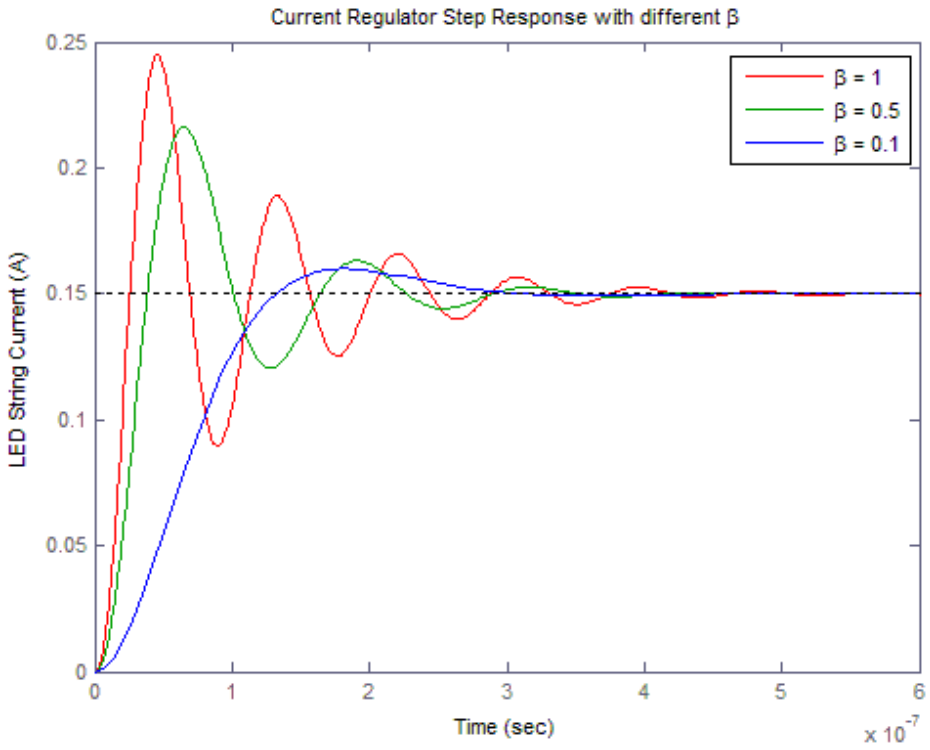

Figure 23. Step response of varying β feedback factors.

The main drawback to gain compensation for this application is the reduction in crossover frequency. In order to provide high dimming ratios, it is desirable for the rise time to be very fast. A design objective of less than 83 ns with minimal overshoot and settling time was originally set. As shown in Figure 23, a β of 0.1 provides a stable step response, but the rise time is beyond 100ns. This is the result of the three poles contained in the transfer function and no zeros to extend the loop bandwidth. Figure 24 demonstrates the crossover frequency reduction due to gain compensation.

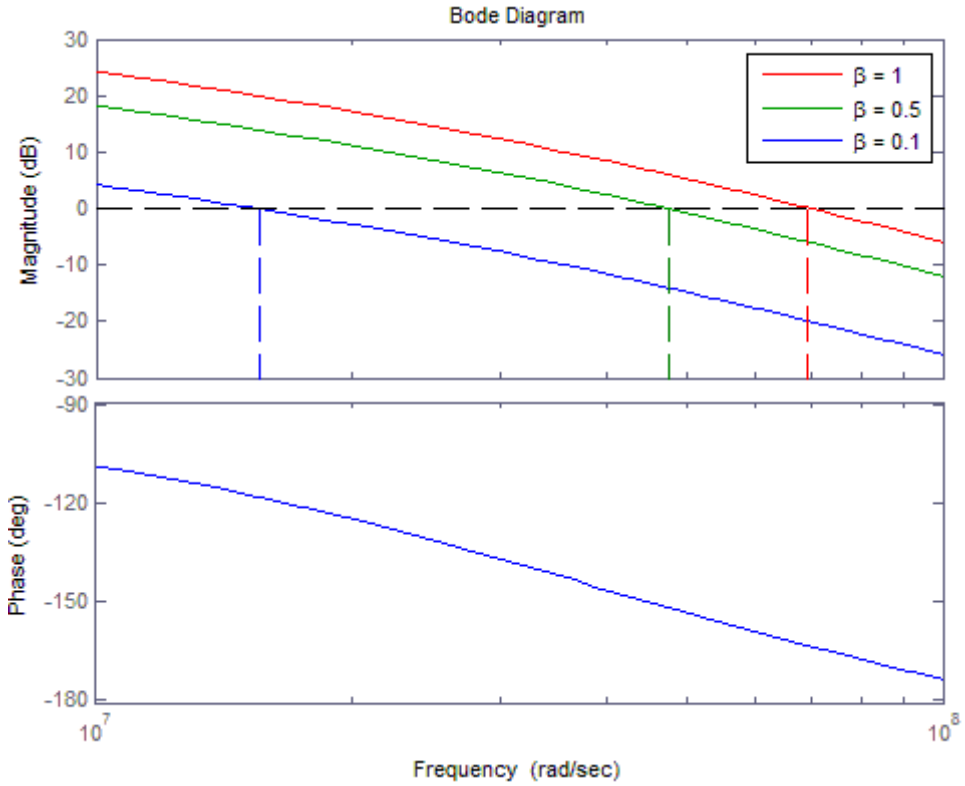

Figure 24. Crossover frequency reduction from gain compensation

3.5.2 Lag Compensation

Lag compensation is used to reduce the loop gain so that crossover occurs at a lower frequency. This is done by adding a pole and zero to the transfer function. The pole is used to increase loop gain roll-off prior to crossover. The zero is placed prior to crossover to provide a positive phase shift to remove the negative phase shift contributed by the lag pole. The realization of a lag network is demonstrated in Figure 25.

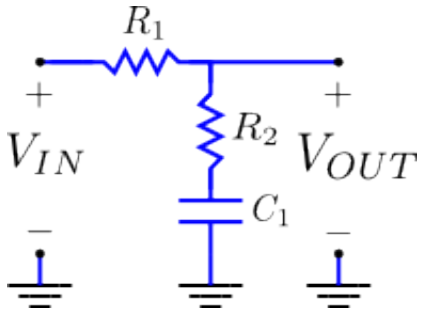

Figure 25. Lag network.

The transfer function of the lag network is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 C_1 \cdot s + 1}{(R_1 + R_2) C_1 \cdot s + 1} \tag{32}$$

where the lag pole is

$$\frac{1}{(R_1 + R_2) C_1} \left({}^{rad}/_{s} \right) \tag{33}$$

and the lag zero is

$$\frac{1}{R_2 \cdot C_1} \left({}^{rad}/_{s} \right) \tag{34}$$

The lag compensation, as shown in Figure 25, can be implemented in either the forward or feedback loop. Figure 26 demonstrates lag compensation in the forward loop.

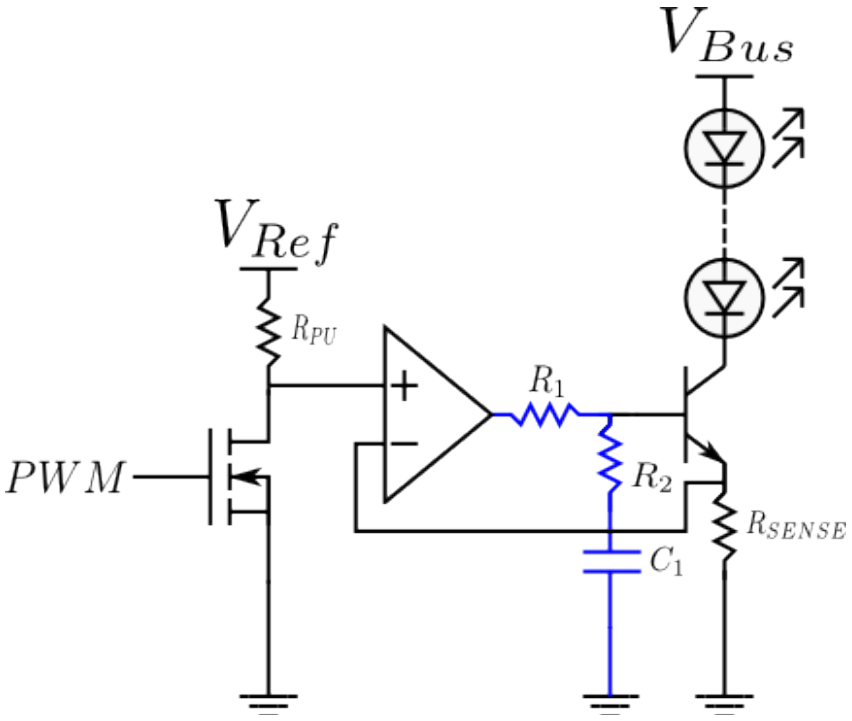

Figure 26. Lag compensation implemented in forward loop.

The major drawback of this topology for this application is that no signal is fed forward. When the lag compensation is implemented in the feedback loop, a phase delay is created, which causes large overshoot issues and non-linearity from saturation of the operational amplifier

output. When lag compensation is implemented in the forward loop, as shown in Figure 26, overshoot issues are removed, but non-linearity issues from saturation of the operational amplifier still exist. Overall, the lag compensation provides poor results for this circuit topology.

3.5.3 Lead Compensation

A lead compensation network provides a positive phase shift in its frequency response. This positive phase shift can be used to extend the crossover frequency of the loop. A lead network realization is shown in Figure 27.

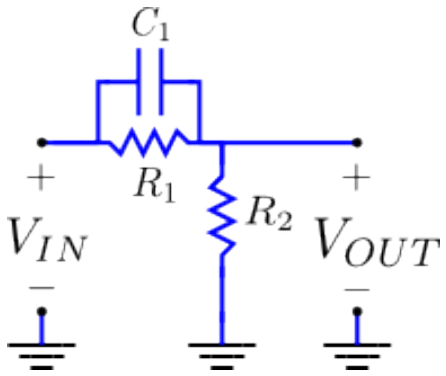

Figure 27. Lead network realization.

The transfer function of the lead network is given by

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{R_2}{R_1 + R_2}\right)\left[\frac{R_1 C_1 \cdot s + 1}{\left(\frac{R_1 \cdot R_2}{R_1 + R_2}\right) C_1 \cdot s + 1}\right] \tag{35}$$

where the lead zero is

$$\frac{1}{R_1 \cdot C_1}\left(rad/s\right) \tag{36}$$

and the lead pole is

$$\frac{1}{\left(\frac{R_1 \cdot R_2}{R_1 + R_2}\right) \cdot C_1}\left(rad/s\right) \tag{37}$$

With DC, the transfer function simplifies down to a resistor divider formed by R_1 and R_2. A current regulator with lead compensation in the feedback loop is shown in Figure 28. A block diagram of the current regulator is provided in Figure 29.

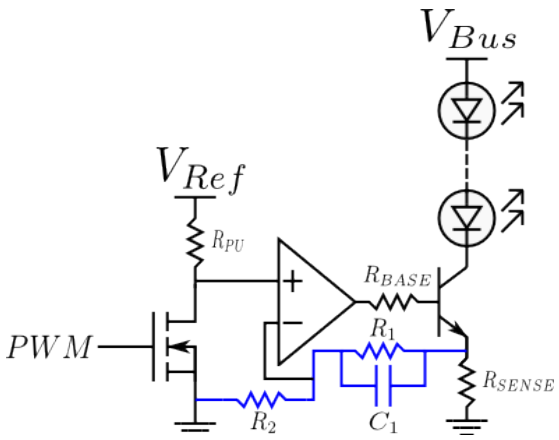

Figure 28. Lead compensation implemented in feedback loop.

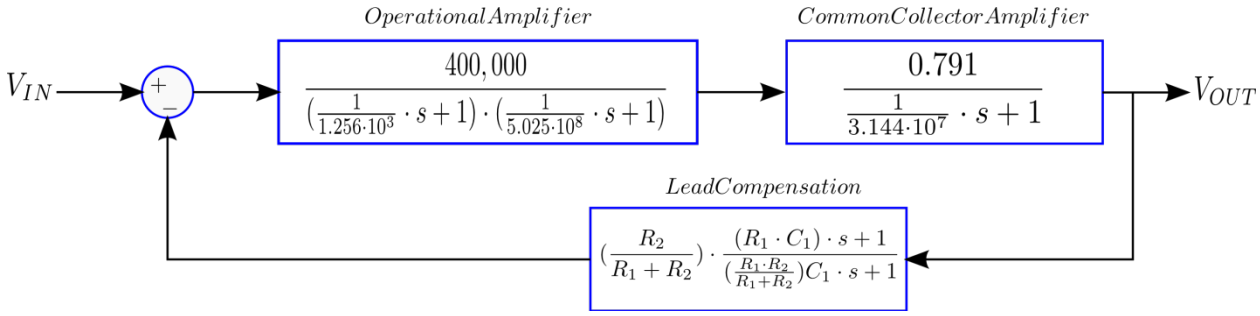

Figure 29. Closed-loop current regulator with lead compensation in feedback loop.

Looking at the closed-loop uncompensated current regulator shown in Figure 29, it can be seen that the first pole encountered in the loop is the low-frequency operational amplifier pole. The second pole is from the common collector amplifier, and the third pole is the high-frequency pole of the operational amplifier. To extend the loop bandwidth, the lead compensator zero-break frequency is placed in the same location as the common collector amplifiers pole. The following resistor and capacitor values are used in the lead compensator:

$$R_1 = R_2 = 316\Omega \tag{38}$$

$$C_1 = 100\text{pF} \tag{39}$$

which yields a closed-loop system, as shown in Figure 30.

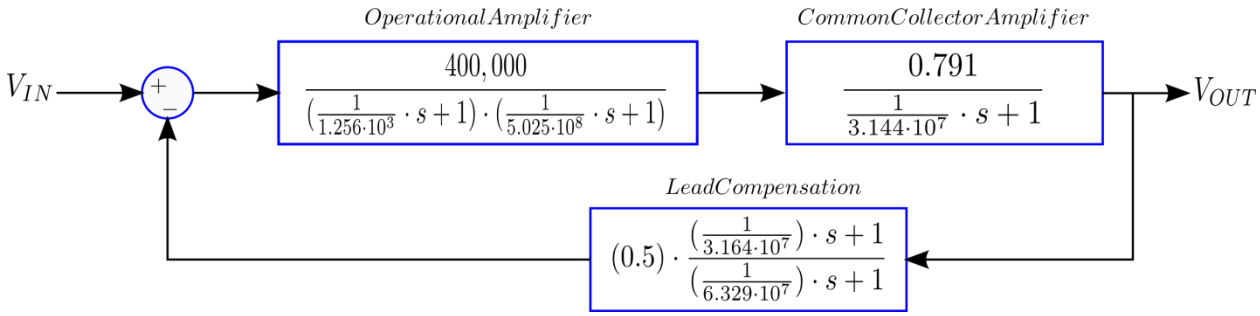

Figure 30. Closed-loop current regulator with substituted values.

The frequency response for a lead compensation network is plotted in Figure 31, and the corresponding phase and gain margins are shown in Figure 32. The step response of the lead compensated current regulator is shown in Figure 33. As can be seen in Figure 33, the rise time is approximately 50 ns with minimal overshoot, which meets the design requirements. The gain and phase margins have been increased to 16.4 dB and 39°, respectively.

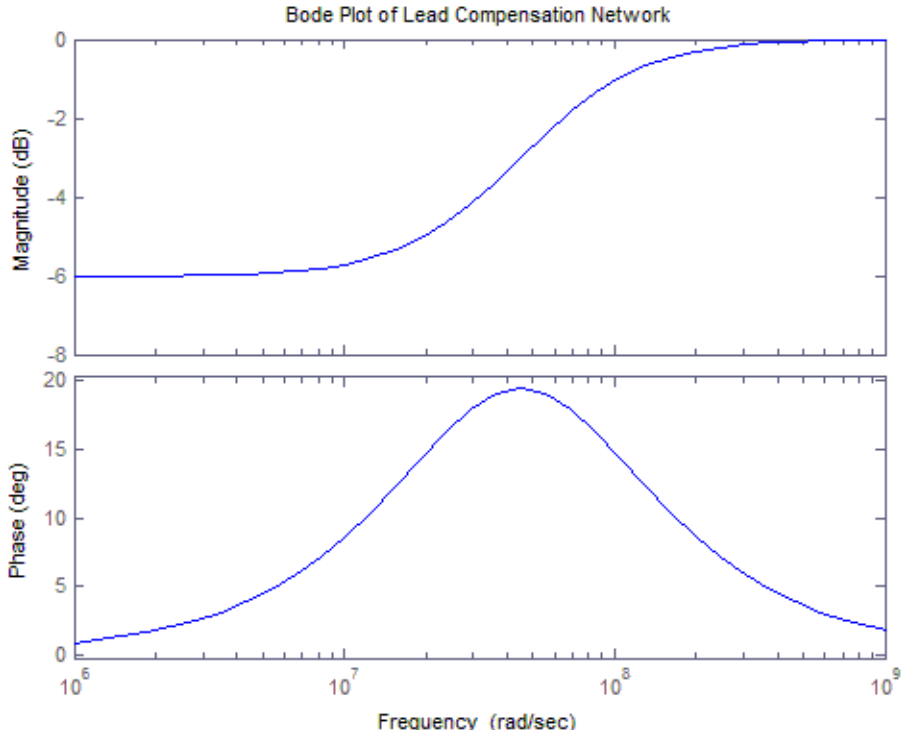

Figure 31. Frequency response of lead compensation network.

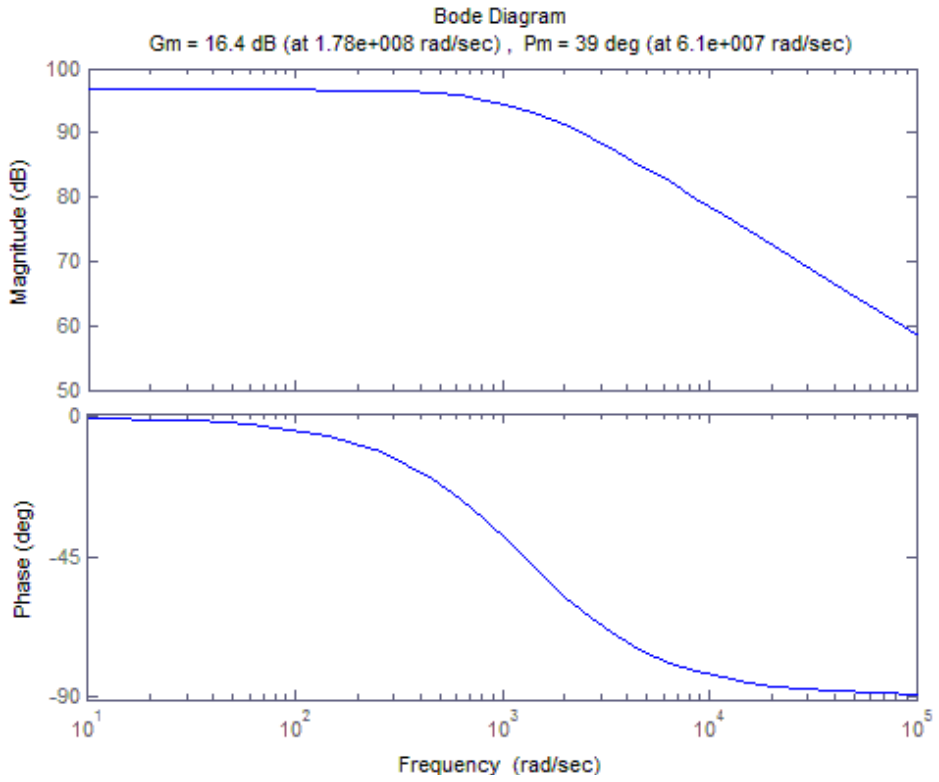

Figure 32. Phase and gain margins of closed-loop lead compensated system.

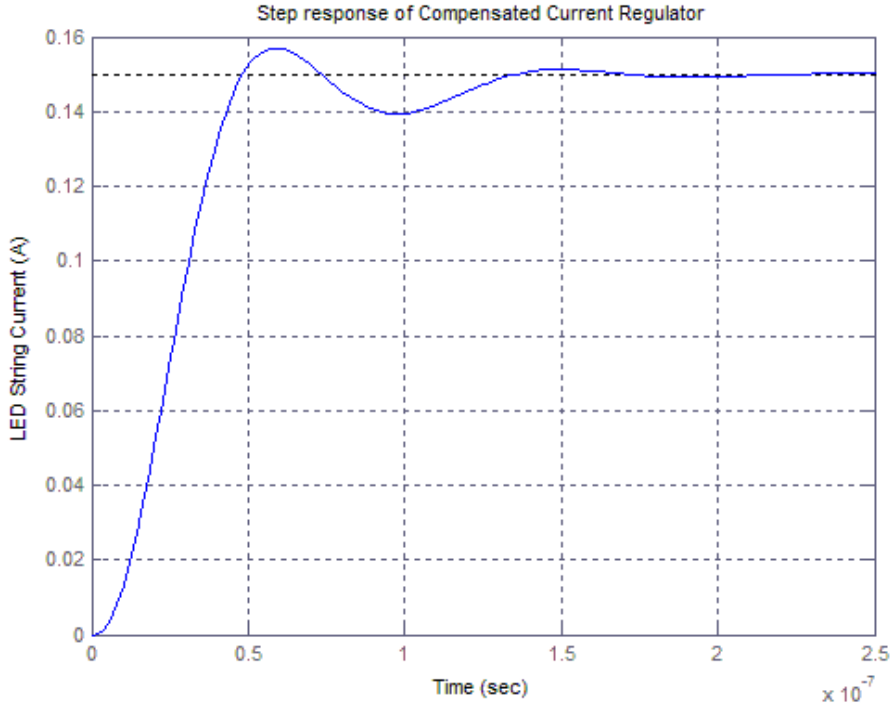

Figure 33. Step response of closed-loop current regulator with lead compensation.

CHAPTER 4

CURRENT REGULATOR SOFT-START

4.1 Current Regulator Soft-Start Overview

The current regulator soft-start circuit is used to reduce the need for a fast transient response power supply. When LEDs are initially turned on, the output voltage of the power supply will begin to drop. The amount of drop is determined by the power supply output capacitance, total LED string current being supplied, and transient response of the power supply. The addition of the soft-start circuit to the system model is shown in Figure 34. Figure 35 demonstrates the addition of the soft-start circuit in the current regulator circuit.

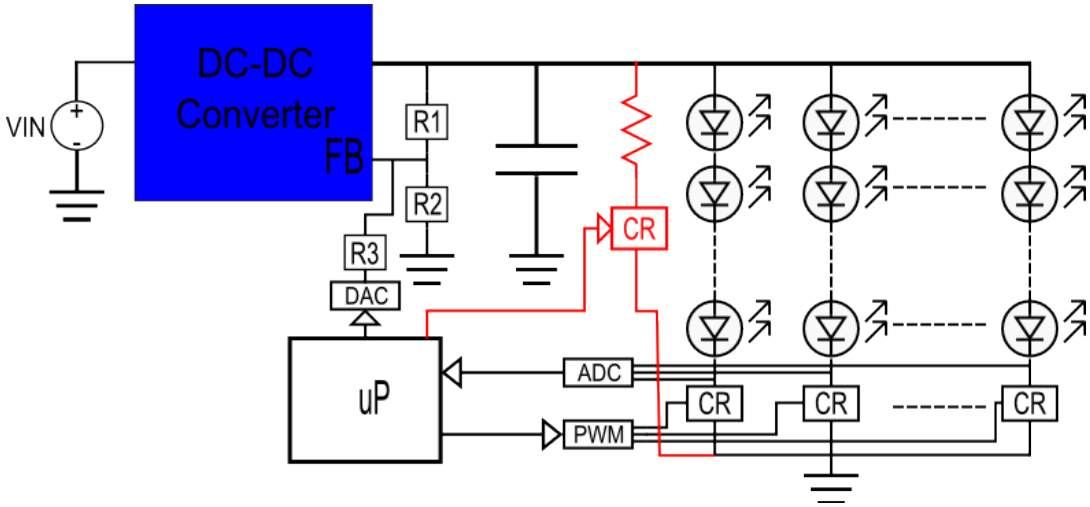

Figure 34. Implementation of soft-start function highlighted in red.

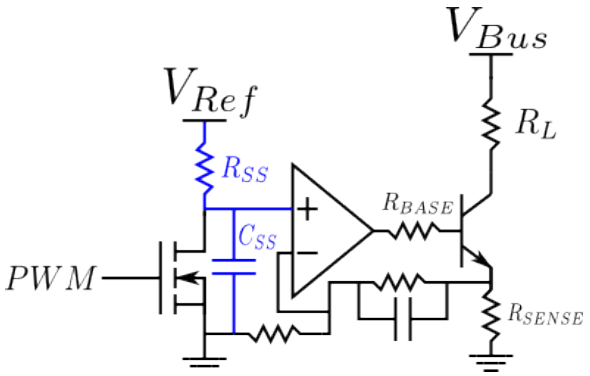

Figure 35. Soft start implemented on a current regulator circuit with a resistive load.

The soft-start circuit is identical to that of the current regulator used for each string, with the addition of a capacitor from the non-inverting input of the operational amplifier to the ground and the LED string replaced with a resistive load.

4.2 Soft-Start Turn-On and Period

When the PWM signal to this circuit is deasserted, the voltage at the non-inverting input of the operational amplifier will begin to increase towards V_{REF}at a rate determined by R_{SS} and C_{SS}. The capacitor voltage waveform for a resistor/capacitor (RC) circuit is shown in Figure 36. Here can be seen the voltage rise on the non-inverting input of the operational amplifier when the PWM signal is deasserted.

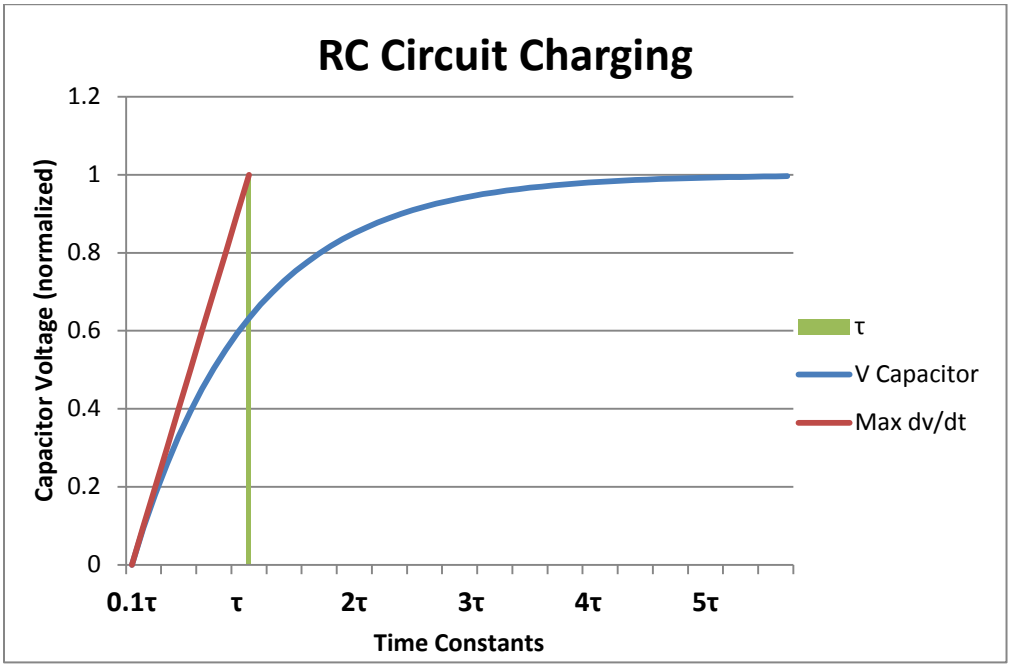

Figure 36. Non-inverting input voltage rise during soft start.

The soft-start current through the current regulator will be proportional to the capacitor voltage:

$$I_{Soft\ Start} = \frac{V_{Capacitor}}{R_{SENSE}} \tag{40}$$

This demonstrates that the circuit can be used to provide an exponential load current ramp, which allows the power supply used to power the circuit to have a much lower transient response since the load current is seen as a ramp rather than a step. To ensure that the output voltage of the power supply will not dip during the soft start, the maximum $\frac{dv}{dt}$ of the voltage on the capacitor, which is proportional to the $\frac{di}{dt}$ of the load, must be less than the transient response of the power supply used. To determine the maximum $\frac{dv}{dt}$ of the resistor and capacitor combination, a differential equation for the charging can be written as

$$\frac{dv_c}{dt} - \left(\frac{1}{RC}\right) v_c = 0 \tag{41}$$

Solving and normalizing the capacitor voltage yields

$$v_{c,norm}(t) = 1 - e^{-t/RC} \tag{42}$$

Taking the derivative and evaluating at $t = 0$ yields the max $\frac{dv}{dt}$. Once the transient response of the power supply is determined, equation (43) will be used to select the resistor and capacitor of the soft-start circuit.

$$\frac{dv_{c,norm}}{dt} = \frac{1}{RC} \tag{43}$$

Then the load current equation for the soft-start circuit is

$$i_{Soft\ Start}(t) = \frac{V_{REF}}{R_{SENSE}}\left(1 - e^{-t/R_{SS}C_{SS}}\right) \tag{44}$$

4.3 Power Supply Transient Response

The transient response of the power supply will be determined by using simulation models, due to the transient response being heavily reliant on power supply architecture, switching frequency, and output capacitance. The power supply used for the analysis is the TPS43060 from Texas Instruments. Simulations are performed in a TINA-TI spice simulator from Texas Instruments. The TPS43060 is setup with a switching frequency of 300kHz. The switching frequency is kept low in order to minimize switching losses and maximize the efficiency of the regulator. The output capacitance of the regulator is 40uF. The ceramic capacitors are simulated with 4x10uF capacitors. No bulk capacitors are used in order to allow for higher power density. The output voltage of the power supply for simulation is set to 28V. The simulation schematic for the TPS43060 device is shown in Figure 37.

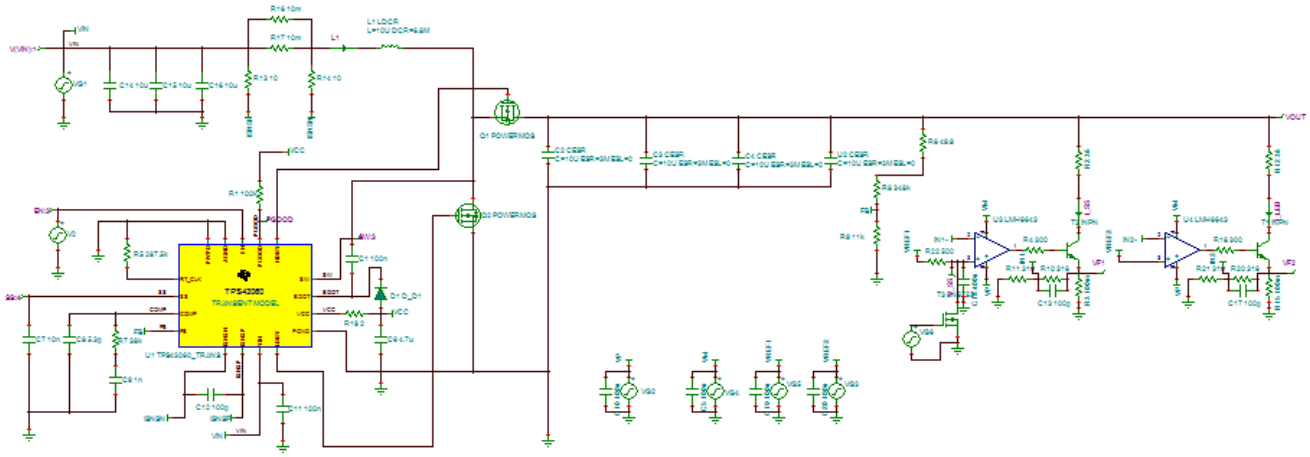

Figure 37. Transient response setup for TPS43060 power supply.

The transient response of the power supply is observed by applying a 1A load current step on the output of the power supply. Figure 38 demonstrates the power supply step response to a 1A load step.

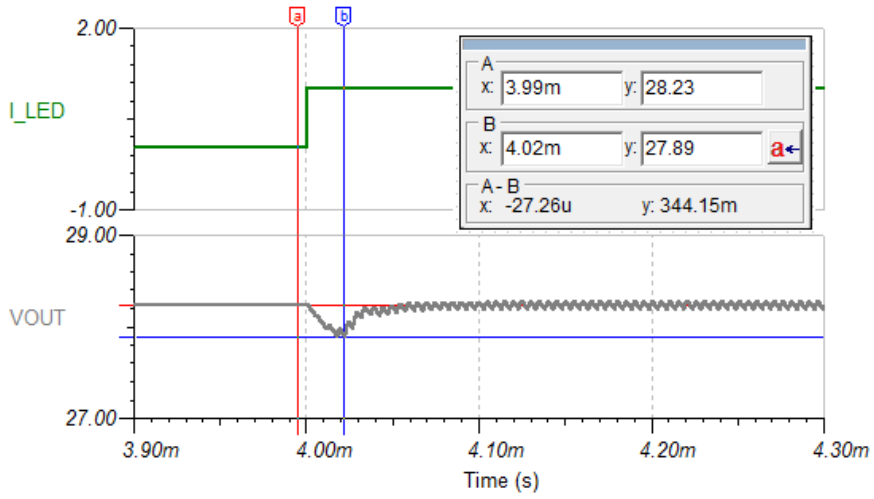

Figure 38. Switching regulator 1A load step response.

As can be seen, the output voltage dips down by ~344mV when the 1A step is initially applied. In the application, any voltage dip from the regulation point reduces the current regulators head room and may cause the current regulator to go out of regulation, which introduces non-linearity into the light output curve. To help reduce the voltage dip seen by the LED current regulators, the soft-start circuit is added. Due to the number of variables that affect the transient response, the soft-start time constant should be determined in the application by varying the time constant until the voltage dip seen by the LED current regulators is removed. The duration of the soft-start circuit is dependent upon the time constant of the selected component values. Table 1 relates the percent charge vs. time constant.

TABLE 1

PERCENT CHARGE VS. TIME CONSTANTS OF RC NETWORK

Percent Charge (%)	Time Constant
63.21	τ
86.47	2τ
95.02	3τ
98.17	4τ
99.33	5τ

A time duration of three time constants will be used for the soft-start circuit. Figure 39 shows that the soft-start current will be ~95% of the desired LED string current at the moment the soft-start circuit is disabled and the LED strings are enabled. Due to the power dissipation that occurs in the soft-start circuit, which will be discussed in section 4.4.1, the soft-start duration should be kept to a minimum to increase overall efficiency. At three time constants and arbitrarily choosing soft-start component values of $R = 500\Omega$ and $C = 4nF$, the circuit will be enabled for~60 µs. .The resulting simulation waveform with the addition of the soft-start circuit is shown in Figure 39.

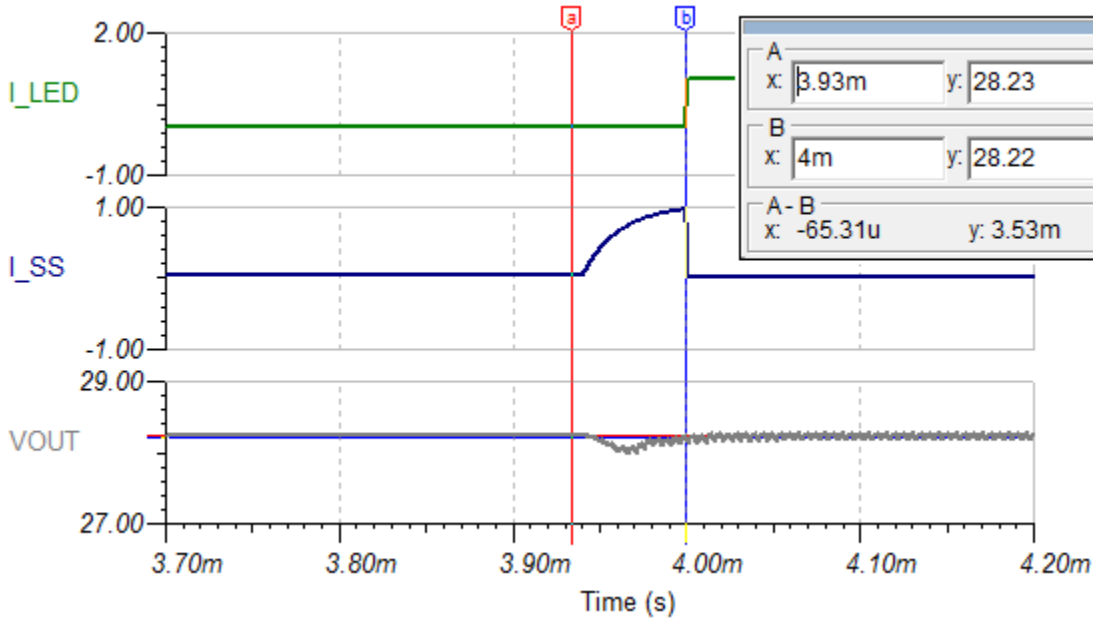

Figure 39. Addition of soft-start circuit.

With the addition of the soft-start circuit, the output voltage initially dips when the soft start is applied but recovers before the soft-start cycle is completed. This demonstrates how the load current is ramped, then at a desired point the soft-start circuit is disabled and the LED string is enabled. At the point where the soft start is disabled and the LED string is enabled, the change in load current is zero, or very small, and the output voltage remains constant. Since the soft-start circuit uses a resistive load rather than LEDs, the light output vs. PWM dimming remains

linear. The result is that the output voltage dip is removed when the LED current regulators are enabled. Because of this, the soft-start circuit has essentially reduced the output voltage dip seen by the current regulators by ~340mV.

4.4 Efficiency Considerations

The goal of the soft-start circuit is to allow an overall higher-efficiency LED driver. However, the power dissipated during the soft-start period must be minimized in order to maximize the overall efficiency gains.

4.4.1 Soft-Start Power Dissipation

The power dissipated during one soft-start cycle of three time constants can be found by

$$P_{SS\_CYCLE} = V_{BUS} \cdot I_{LED} \int_0^{3\tau} \left(1 - e^{-t/RC}\right) \cdot dt \tag{45}$$

After solving the integral,

$$P_{SS\_CYCLE} = V_{BUS} \cdot I_{LED} \left(3\tau + RC\left(e^{-3\tau/RC} - 1\right)\right) \tag{46}$$

where $\tau = RC$:

$$P_{SS\_CYCLE} = V_{BUS} \cdot I_{LED}\left(3 \cdot RC + RC(e^{-3} - 1)\right) \tag{47}$$

The number of times the soft start operates in a one-second period is equal to the PWM frequency. As the PWM frequency is increased, the overall efficiency will decrease. Figure 40 relates system efficiency to PWM frequency, demonstrating the tradeoff between PWM frequency and efficiency. The PWM frequency should be kept sufficiently low to yield acceptable efficiency. Figure 41 relates system efficiency to the PWM duty cycle at 120Hz dimming.

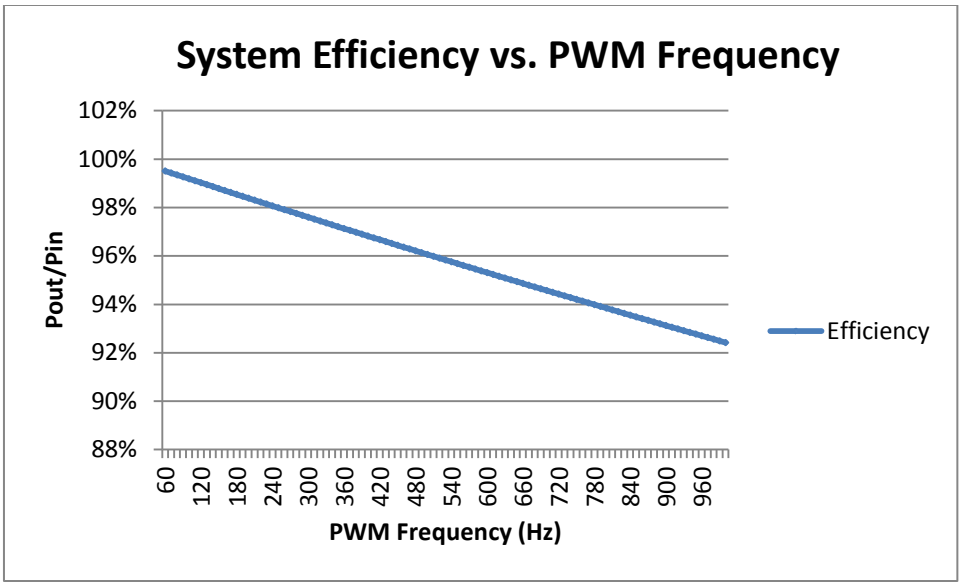

Figure 40. System efficiency vs. PWM frequency with 60µs soft start at 50% duty cycle.

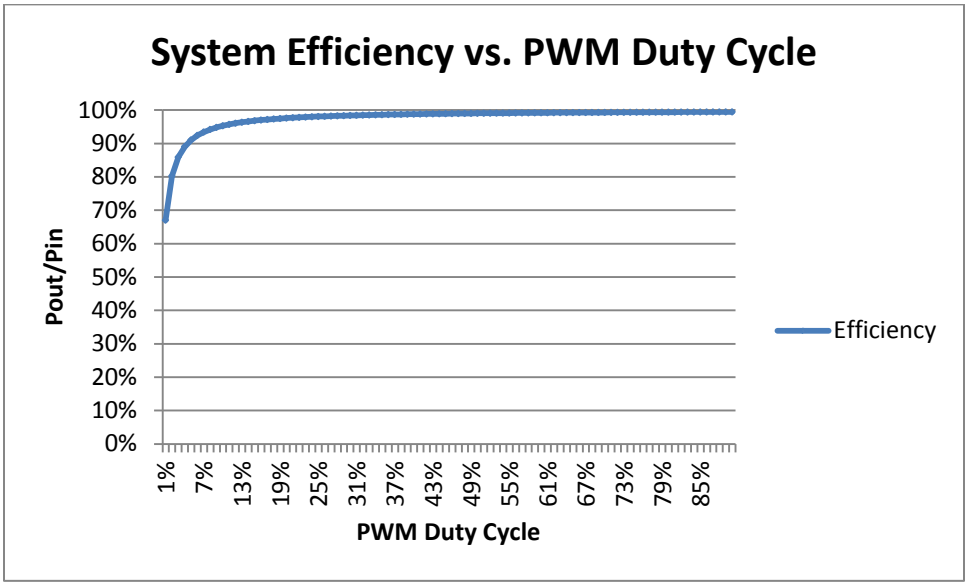

Figure 41. Efficiency vs. PWM duty cycle at 120Hz.

Since the soft-start turn-on remains constant at varying PWM duty cycles, the overall system efficiency will decrease at low-duty cycle values. Even though the efficiency is reduced during low-duty cycle operation, the actual power dissipation from the soft start is low. For example, when operating under the following conditions, the power dissipation is minimal and

can be regained in the reduced head room requirements that are obtained with the soft-start circuit:

- 120Hz PWM
- $I_{LED} = 1A,\ V_{LED} = 28V$
- $t_{SS} = 60us$

$$P_{Dis} = P_{SS\_CYCLE} * 120Hz = 28V \cdot 1A\left(3 \cdot 500 \cdot 40e^{-9} + 500 \cdot 40e^{-9}(e^{-3} - 1)\right) = 0.14W$$

4.4.2 Efficiency Gains

As demonstrated in section 4.3, with a 60µs soft start incorporated, the output voltage dip decreased by 340mV. This reduced voltage dip allows the current regulator to run at a reduced head room voltage (V_{HR}) without losing regulation when the LEDs are initially turned on. Figure 42 defines the V_{HR} of the current regulator circuit.

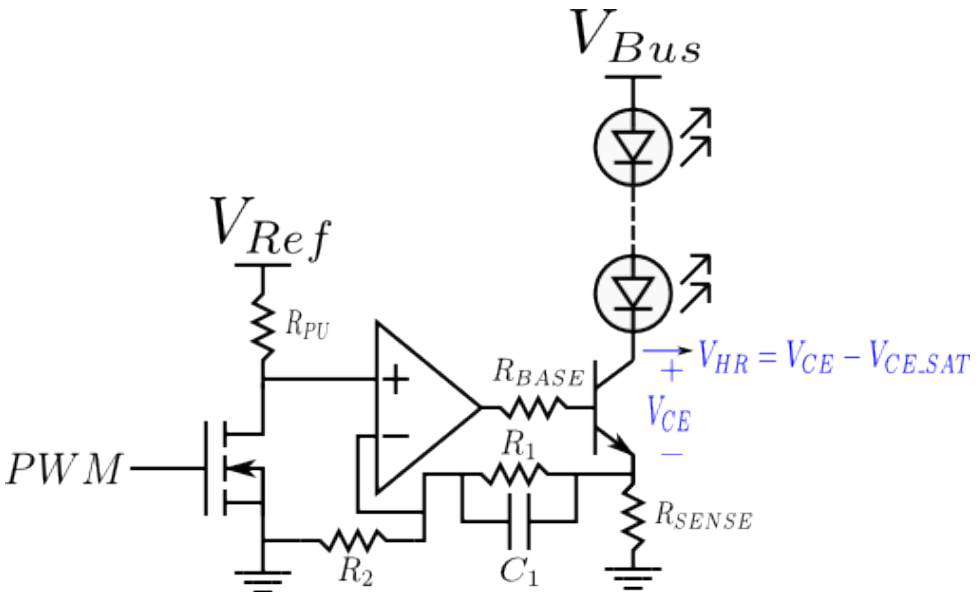

Figure 42. Headroom voltage of LED constant current regulator.

Some amount of headroom must be kept to ensure that the regulator is able to maintain a constant current; however, excessive headroom reduces efficiency of the regulator. The required amount of headroom is dependent upon the amount of output voltage dip that occurs when the

LEDs are initially turned on. Turn-on exhibits the worst-case situation since load goes from zero to full. The excess power lost in each LED string from the head room is

$$P_{HR} = V_{HR} * I_{LED} \tag{48}$$

which is representative of the power lost in each LED string within the system. In section 4.3, it was demonstrated that with the use of a 60µs soft-start period, the output voltage dip was reduced by ~340mV, which allows the required head room to be reduced by the same amount. The power savings from this reduced head room will be greater with higher duty-cycle PWM values:

$$P_{Reduction} = (HR_{Reduction} \cdot I_{LED}) \cdot D_{PWM} \tag{49}$$

Figure 43 relates head room power savings to the PWM duty cycle. The overall power reduction related to PWM duty cycle is given in Figure 44. As can be seen, at a low PWM duty cycle, the soft-start losses overtake the head room gains. The system should be designed to average above an ~50% duty cycle to benefit from soft-start gains. Further efficiency gains will also be seen from the reduced switching frequency that the soft-start circuit allows.

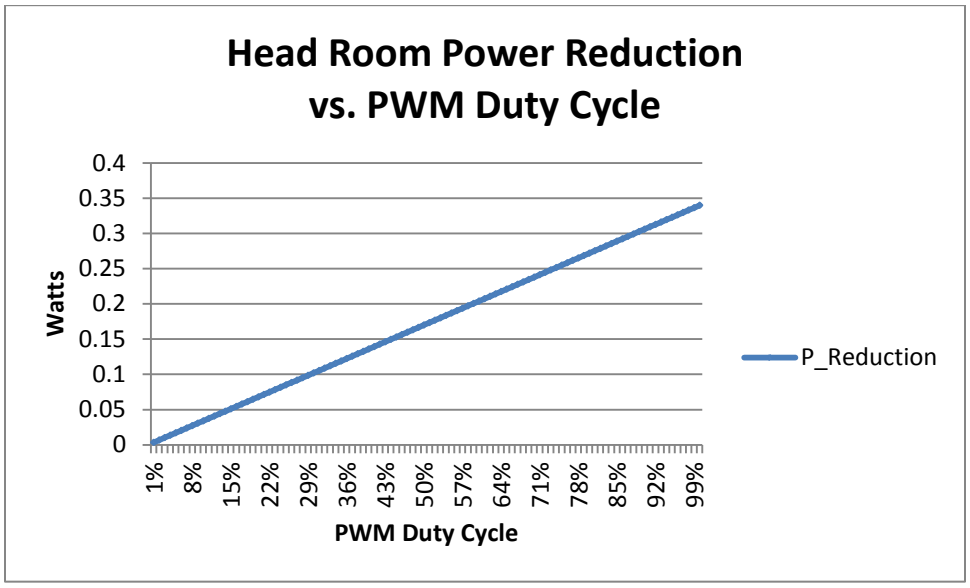

Figure 43. System power reductions from reduced head room without accounting for soft-start losses.

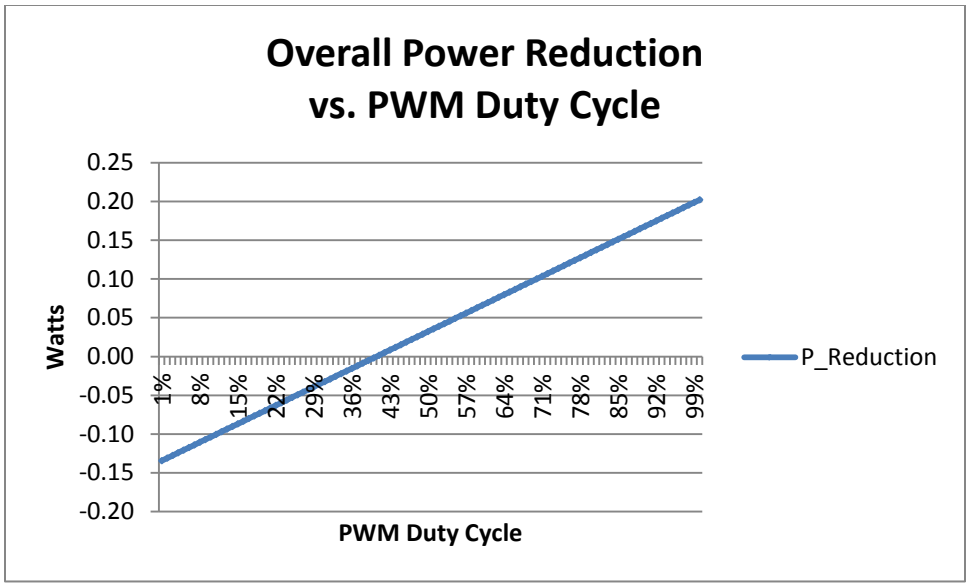

Figure 44. Overall power reductions accounting for soft start and head room.

CHAPTER 5

CURRENT REGULATOR HEAD ROOM ADJUSTMENT

5.1 Head Room Adjustment Overview

Head room adjustment is the process of minimizing the excess voltage drop across the current regulator, as shown in Figure 45. Without this adjustment, the efficiency of the regulator will not be optimized. The head room adjustment circuit utilizes an analog-to-digital converter to measure the potential at the collector of the pass transistor in the current regulator circuit. The ADC data is then used to adjust the output bus voltage until a defined voltage is reached at the collector of the current regulator. Algorithms for open-string detection or shorted LED detection are not considered in this thesis.

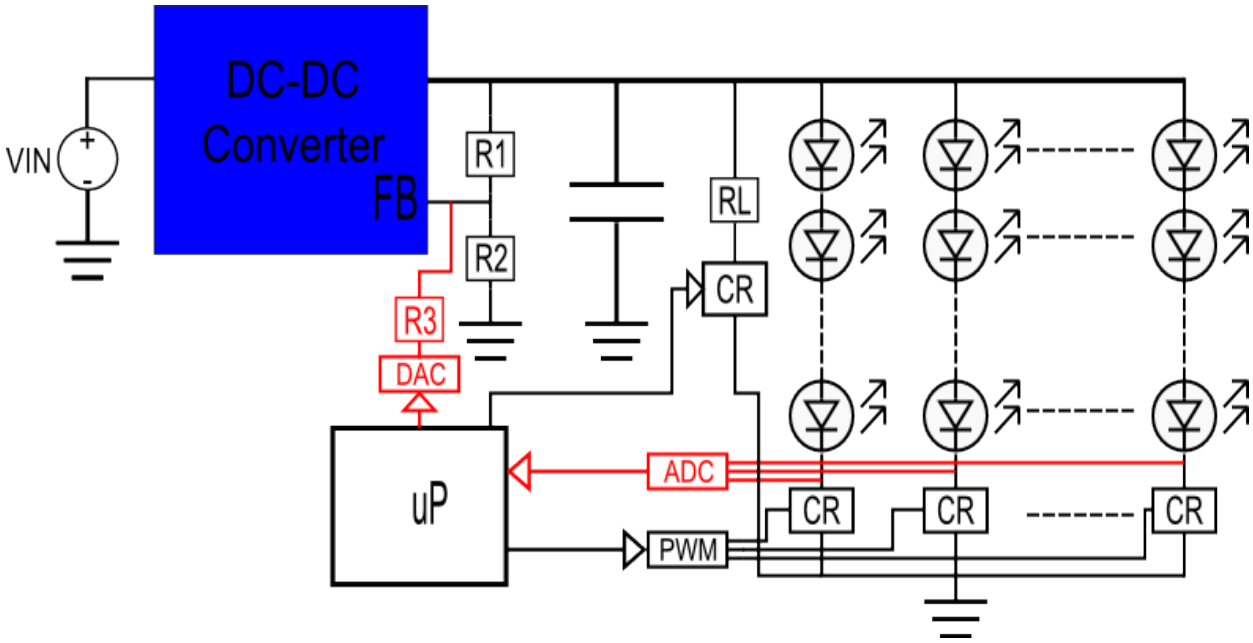

Figure 45. Implementation of head room adjustment function highlighted in red.

5.2 ADC Measurements for Head Room

The analog-to-digital converter measurements used to determine the head room adjustment are made on a PWM cycle basis, where *N* LED strings are measured in *N* PWM

cycles. Figure 46 demonstrates the sequential string ADC measurements used for the head room adjustment. It is assumed that LED forward-voltage changes occur at a very slow rate. Under this assumption, the ADC measurement and head room adjustment sequence can be run periodically and does not need to run constantly. Due to the relatively slow PWM period relative to ADC data transfer, a simple serial ADC can be used. To measure during low PWM duty cycles, a sample and hold circuit can be utilized to allow the use of ADC's with longer conversion times.

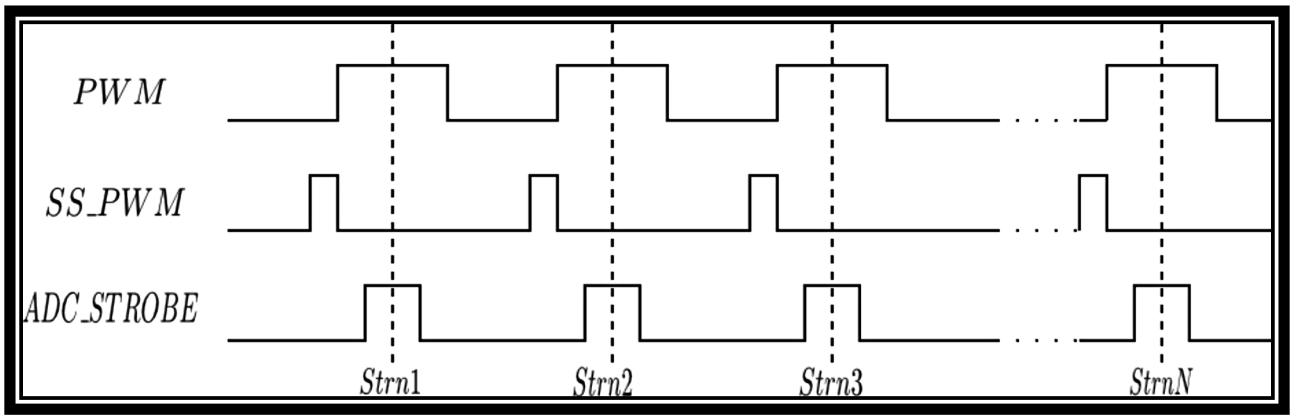

Figure 46. ADC measurements on PWM cycle basis.

5.3 Output Adjustment Circuit

The output adjustment circuit is implemented by utilizing the feedback loop of the DC-DC converter and adding a third resistor to the feedback node along with a digital-to-analog converter (DAC) to allow adjustment for the LED supply voltage. Figure 47 shows the output adjustment circuit with the terminals labeled, and Figure 48 shows a block diagram of the system with the regular DC-DC converter control loop and an additional control loop for head room adjustments.

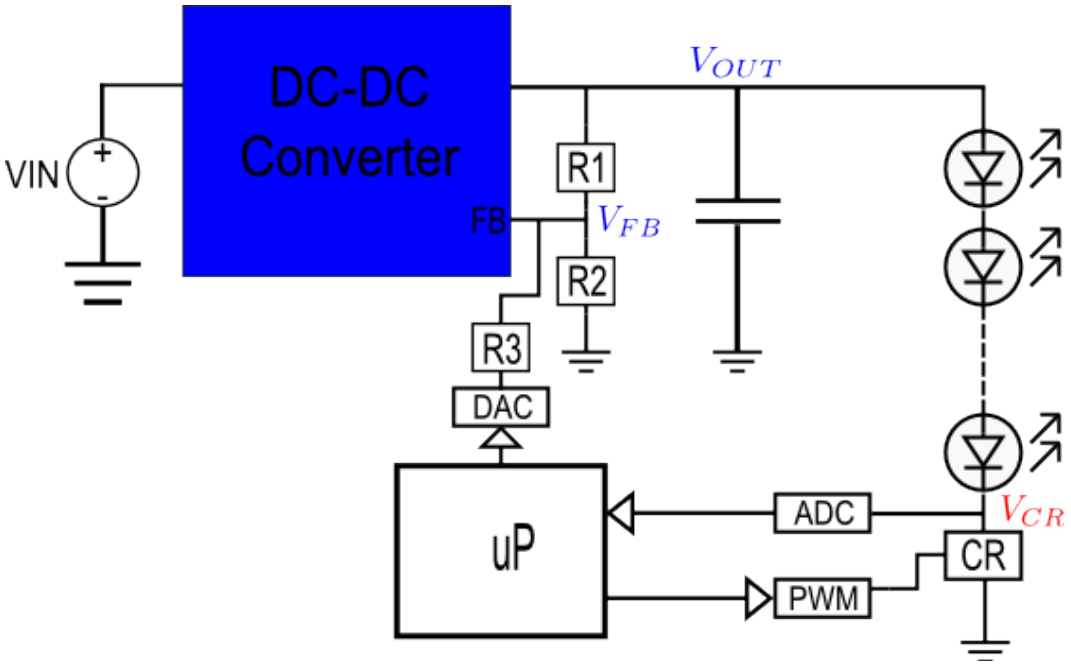

Figure 47. Output adjustment circuit with a single LED string.

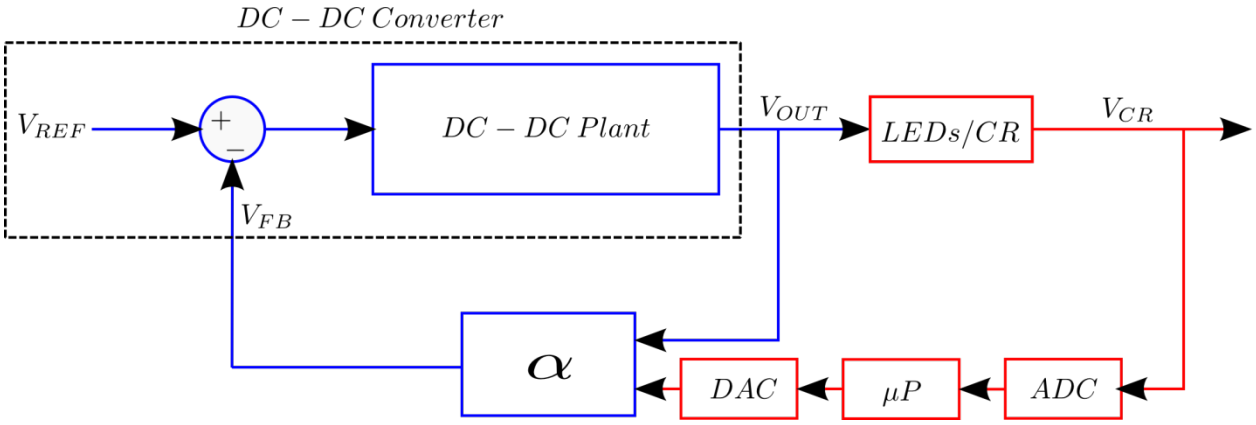

Figure 48. Block diagram of system with regular DC-DC converter control loop highlighted in blue and additional control loop for head room adjustments highlighted in red.

First, considering the DC-DC converter feedback loop highlighted in blue, the feedback factor α, is a constant value that does not vary with time. The purpose of the added portion of the control loop highlighted in red is to vary the value of α, which in turn will vary the output voltage to achieve the desired value V_{CR}. Figure 49 demonstrates the circuit used for α adjustment.

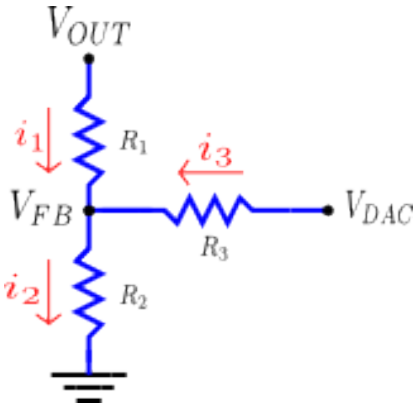

Figure 49. Resistor network used for α adjustment.

The DC-DC converter regulates the V_{FB} node to the reference voltage contained within the regulator, the value of which is provided in the manufacturer's datasheet. Since the V_{FB} is regulated and remains constant in steady state, the current i_2 remains constant. When V_{DAC} is set to a potential above the reference voltage V_{FB}, a current i_3 flows into the V_{FB} node. Since i_2 is constant, V_{OUT} must be reduced, which in turn reduces the magnitude of i_1 by an amount i_3; therefore, Kirchhoff's current law is satisfied. Similarly, when V_{DAC} is set to a potential below that of V_{FB}, the current i_3 becomes negative and flows out of the V_{FB} node. For i_2 to remain constant, V_{OUT} must increase. The effects of V_{DAC} and R_3on the output voltage are shown by

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) + \frac{R_1}{R_3} \cdot (V_{FB} - V_{DAC}) \tag{50}$$

which in turn shows that if $V_{DAC} = V_{FB}$, then V_{OUT} is unaffected by the output adjustment circuitry. The DAC reference voltage will be set as

$$V_{DAC\_REF} = 2 * V_{FB} \tag{51}$$

which allows the full-scale range of V_{DAC} to be

$$0 \leq V_{DAC} \leq 2 * V_{FB} \tag{52}$$

The value of R_3 can then be used to determine the amount of output voltage adjustment that the system can achieve. For example, given the following parameters:

- $V_{OUT} = 28V\ nominal, desired\ to\ actuate\ between\ 26V\ to\ 30V$
- $V_{FB} = 1.22V\ (from\ TPS43060\ datasheet)$
- $V_{DAC}\ output\ voltage\ range\ is\ 0 \leq V_{DAC} \leq 2.44V$
- $R_1 = 887k\Omega$
- $R_2 = 40.41k\Omega\ (37.4k\Omega + 3.01k\Omega)$

the value of R_3 can then be determined from

$$R_3 = \frac{R_1 \cdot \left(V_{FB} - V_{DAC\_MAX}\right)}{V_{OUT\_MIN} - V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right)} = \frac{887k\Omega \cdot (1.22V - 2.44V)}{26V - 1.22V \cdot \left(1 + \frac{887k\Omega}{40.41k\Omega}\right)} \cong 541k\Omega \qquad (53)$$

Given that the V_{DAC} range is centered about V_{FB}, and the nominal value of V_{OUT} is centered between minimum and maximum actuation points, an equally valid calculation method would be

$$R_3 = \frac{R_1 \cdot \left(V_{FB} - V_{DAC\_MIN}\right)}{V_{OUT\_MAX} - V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right)} = \frac{887k\Omega \cdot (1.22V - 0V)}{30V - 1.22V \cdot \left(1 + \frac{887k\Omega}{40.41k\Omega}\right)} \cong 541k\Omega \qquad (54)$$

For implementation of the output adjustment algorithm, the output voltage is first determined using equation (50). Next, the optimal output voltage is found by

$$V_{OUT\_OPTIMAL} = V_{OUT} - \left(V_{ADC} - V_{ADC\_OPTIMAL}\right) \qquad (55)$$

Where V_{ADC} is the measured head room voltage of the current regulator and $V_{ADC\_OPTIMAL}$ is the target head room voltage. Finally, solving equation (50) for V_{DAC} and substituting in $V_{ADC\_OPTIMAL}$ yields the new set value of V_{DAC}

$$V_{DAC} = \frac{R_3}{R_1}\left(V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) - V_{OUT\_OPTIMAL}\right) + V_{FB} \qquad (56)$$

The value $V_{ADC\_OPTIMAL}$ is determined by the selected value of R_{SENSE} and saturation voltage of the pass transistor used for the current regulator. The final value should be determined through experimental testing of the application. Figure 50 demonstrates the output voltage adjustment with respect to the V_{DAC} voltage.

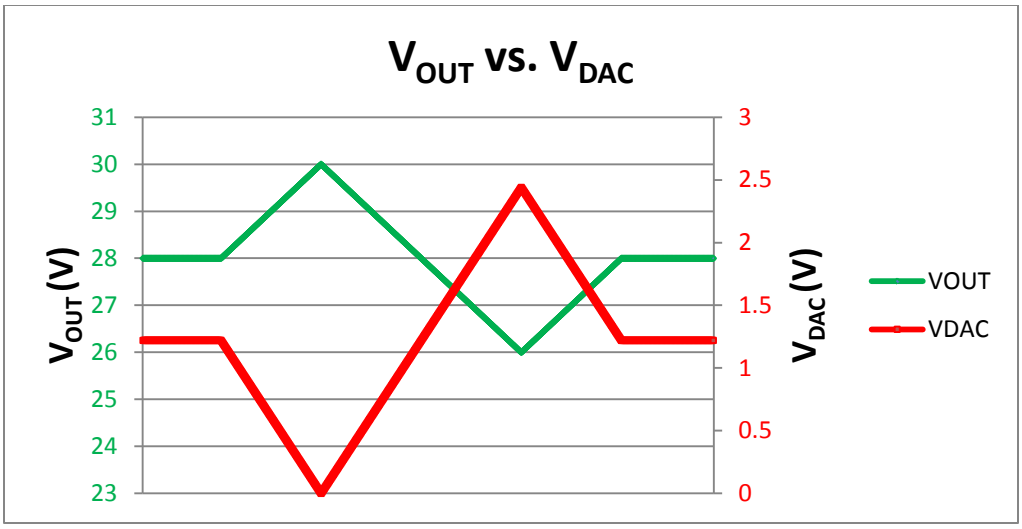

Figure 50. Output voltage adjustment waveforms.

CHAPTER 6

CONCLUSION

The work presented in this thesis demonstrates the system building blocks that can be utilized in designing an LED driver with a high dimming ratio. The system architecture utilizes common components that can be easily exchanged to help alleviate obsolescence issues in applications where long product life support is required. A current regulator circuit topology is presented to achieve a fast LED current rise time, which allows for an increase in the dimming ratio. A soft-start circuit topology was demonstrated to ramp the LED current, which effectively allows a decrease in required head room and overall increase in efficiency. Finally, a headroom adjustment circuit was shown to allow an output voltage adjustment that can be utilized with many off-the-shelf switching power supplies.

Future research would include investigating other methods of utilizing the deterministic nature of the system to perform the soft start function without dissipating the power into a resistive load. This would result in further efficiency increases.

REFERENCES

REFERENCES

[1] Novitsky, Tom, and Abbott, Bill, “Driving LEDs versus CCFLs for LCD backlighting,” *EE Times*, Endicott Research Group, Inc., November 12, 2007,URL: http://www.eetimes.com/document.asp?doc_id=1272405[cited September 13, 2014].

[2] Gu, Y., Narendran, N., Dong, T., and Wu, H., “Spectral and luminous efficacy change of high-power LEDs under different dimming methods,” *Proceedings of SPIE Sixth International Conference on Solid State Lighting*, Vol. 6337, 2006.

[3] Hong, S., Han, J., Kim, D., and Kwon, D., “A double-loop control LED backlight driver IC for medium-sized LCDs,” *IEEE International Solid-State Circuits Conference*, February 7–11, 2010, pp.116–117.

[4] Hu, Y., and Jovanovic, M., “LED driver with self-adaptive drive voltage," *IEEE Transactions on Power Electronics*, Vol. 23, No.6, November 2008, pp.3116–3125.

[5] Doshi, M. and Zane, R., “Digital architecture for driving large LED arrays with dynamic bus voltage regulation and phase shifted PWM,” *IEEE Applied Power Electronics Conference*, February 25, 2007–March 1, 2007, pp. 287–293.

[6] Hsieh, Y., Liu, B., Wu, J., Fang, C., Tsai, H., and Juang, Y., “A high-dimming-ratio LED driver for LCD backlights,” *IEEE Transactions on Power Electronics*, Vol. 27, No.11, November 2012, pp.4562, 4570.

[7] Xu, X., and Wu, X., “High dimming ratio LED driver with fast transient boost converter,” *IEEE Power Electronics Specialists Conference*, June 15-19, 2008, pp.4192–4195.

[8] MAXIM Integrated Products, Inc., Datasheet: MAX17061, “8 string white LED driver with SMBus for LCD panel applications,”2008.

[9] Analog Devices Inc., Datasheet: ADD5211, “Four-string, white LED Driver for LCD backlight applications, 2013.

[10] Feng, D., Singh, P., and Sandborn, P., “Lifetime buy optimization to minimize lifecycle cost,” *Proceedings of the Aging Aircraft Conference*, 2007.

APPENDICES

APPENDIX A

MATLAB CODE FOR CHAPTER 2

Code for Figure 2:

```
% Low-frequency poles
lp=100;
lf_pole=[1/(2*pi*lp) 1];

% High-frequency poles
hp1=200e3;
hp2=300e3;
hf1_pole=[1/(2*pi*hp1) 1];
hf2_pole=[1/(2*pi*hp2) 1];

% Transfer function
denom=conv(lf_pole, hf1_pole);
denom1=conv(denom, hf2_pole);
aol=10^(3/20)*(hp1/lp);
tfunc_opa=tf(aol, denom1);

% Gain/phase margin
margin(tfunc_opa)
```

Code for Figure 3:

See Appendix B, Figure 19.

Code for Figure 4:

```
% Lead compensation network
R1 = 200e3;
R2 = 1e3;
C1 = 1e-6;

% Transfer function
num = [R1*R2*C1, R2];
den = [R1*R2*C1, R1+R2];
t_func = tf(num, den);

% Bode plot
bode(t_func)
```

Code for Figure 5:

```
% Lag compensation network
R1 = 200e3;
R2 = 1e3;
C1 = 1e-6;

% Transfer function
num = [R2*C1, 1];
den = [C1*(R1+R2), 1];
t_func = tf(num, den);

% Bode plot
bode(t_func)
```

APPENDIX B

MATLAB CODE FOR CHAPTER 3

Code for Figures 10, 12, 16, 17, 31, 32, and 33:

```
RSENSE = 1;    % Emitter sense resistor
fT = 500e6;    % Unity gain transistor frequency
RBIAS = 300;   % Base bias resistance
VT = 25e-3;    % Transistor thermal voltage (at 25°C)
IC = 150e-3;   % LED string current
GM = IC / VT; % Transistor transconductance
Hfe = 100;     % Transistor DC gain
R_PI = (Hfe * VT) / IC;  % Base resistance

% Lead compensation network parameters
RIN = 316;
CIN = 100e-12;
ROUT = 316;

% Op-amp transfer function
lp = 200;  %Hz, dominant pole
hp = 80e6; %Hz, high-frequency pole
lf_pole = [1/(2 * pi * lp)  1];
hf_pole = [1/(2 * pi * hp) 1];
denom = conv(lf_pole, hf_pole);
aol = 10^(3 / 20) * (hp / lp);  % Account for 3dB error.
Tfunc_opa = tf(aol, denom);
bode(Tfunc_opa, {1, 1e11});
title('Gm=Inf dB (at Inf rad/sec), Pm=45 deg (at 5.02e+008 rad/sec)')

% Common collector amplifier
Ao = ((1 + Hfe)* RSENSE) / ((1 + Hfe) * RSENSE + RBIAS + R_PI);
denom = [Hfe / (2 * pi * fT), 1];
Tfunc_bjt = tf(Ao, denom);
[z,p,k] = zpkdata(Tfunc_bjt);
z;
p;
k;
figure;
bode(Tfunc_bjt, {1, 1e11});
title('Frequency response of common collector amplifier')

% Loop transmission of system
Loop = Tfunc_opa * Tfunc_bjt;
```

```
figure;
margin(Loop);

% Closed-loop system
c_loop = feedback(Loop, 1);
figure;
step(0.150 * c_loop);
grid;
title('Step response of current regulator')
ylabel('LED string current (A)')

% Lead compensation
num = [RIN * CIN, 1];
denom = [(RIN * ROUT * CIN) / (RIN + ROUT), 1];
comp = tf(num, denom);
Tfunc_comp = (ROUT / (RIN + ROUT)) * comp;
figure;
bode(Tfunc_comp);
title('Bode plot of lead compensation network')
c_loop = feedback(Loop, Tfunc_comp)
figure;
step(0.075 * c_loop);
grid;
title('Step response of compensated current regulator')
ylabel('LED string current (A)')

% Loop transmission of compensated system
Loop = Tfunc_opa * Tfunc_bjt * Tfunc_comp;
figure;
margin(Loop);
```

Code for Figures19 and 20:

```
RSENSE = 1;    % Emitter sense resistor
fT = 500e6;    % Unity gain transistor frequency
RBIAS = 300;   % Base bias resistance
VT = 25e-3;    % Transistor thermal voltage (at 25°C)
IC = 150e-3;   % LED string current
GM = IC / VT; % Transistor transconductance
Hfe = 100;     % Transistor DC gain
ROUT = 0;      % Output resistance of op-amp
R_PI = (Hfe * VT) / IC;  % Base resistance
```

```
% Op-amp transfer function
lp = 200;  %Hz, dominant pole
hp = 80e6; %Hz, high-frequency pole
lf_pole = [1/(2 * pi * lp)  1];
hf_pole = [1/(2 * pi * hp) 1];
denom = conv(lf_pole, hf_pole);
aol = 10 ^ (3 / 20) * (hp / lp);  % Account for –3dB error.
Tfunc_opa = tf(aol, denom);

% Gain compensation using R_BASE
Loop_gc = tf(zeros(1, 1, 3, 3));
cl_gc = tf(zeros(1, 1, 3, 3));
R_Base = [300, 600, 900];
for i = 1 : length(R_Base)
   Ao = ((1 + Hfe)* RSENSE) / ((1 + Hfe) * RSENSE + R_Base(i) + R_PI);
   denom = [Hfe / (2 * pi * fT), 1];
   Tfunc_bjt = tf(Ao, denom);
   Loop_gc(:, :, 1, i) = Tfunc_opa * Tfunc_bjt;
   cl_gc(:, :, 1, i) = feedback(Tfunc_opa * Tfunc_bjt, 1);
end

figure;
bode(Loop_gc(:, :, 1, 1),'r',Loop_gc(:, :, 1, 2),'g',Loop_gc(:, :, 1, 3),'b')
axes_handles = findall(gcf, 'type', 'axes');
legend(axes_handles(3), ['R_{Base} = ' num2str(R_Base(1)) '\Omega'], ['R_{Base} = '
num2str(R_Base(2)) '\Omega'], ['R_{Base} = ' num2str(R_Base(3)) '\Omega'], 'Location',
'Southwest');
title('Loop gain vs. base resistance')

figure;
step(0.15 * cl_gc(:, :, 1, 1),'r', 0.15 * cl_gc(:, :, 1, 2),'g', 0.15 * cl_gc(:, :, 1, 3),'b')
axes_handles = findall(gcf, 'type', 'axes');
legend(axes_handles(2), ['R_{Base} = ' num2str(R_Base(1)) '\Omega'], ['R_{Base} = '
num2str(R_Base(2)) '\Omega'], ['R_{Base} = ' num2str(R_Base(3)) '\Omega'], 'Location',
'Northeast');
ylabel('LED string current (A)')
title('Current regulator step response')
```

Code for Figures 22, 23, and 24:

```
RSENSE = 1;    % Emitter sense resistor
fT = 500e6;    % Unity gain transistor frequency
RBIAS = 300;   % Base bias resistance
```

```
VT = 25e-3;    % Transistor thermal voltage (at 25°C)
IC = 150e-3;   % LED string current
GM = IC / VT;  % Transistor transconductance
Hfe = 100;     % Transistor DC gain
ROUT = 0;      % Output resistance of op-amp
R_PI = (Hfe * VT) / IC;  % Base resistance

% Op-amp Transfer Function
lp = 200;  %Hz, dominant pole
hp = 80e6; %Hz, high-frequency pole
lf_pole = [1/(2 * pi * lp)  1];
hf_pole = [1/(2 * pi * hp) 1];
denom = conv(lf_pole, hf_pole);
aol = 10 ^ (3 / 20) * (hp / lp);  % Account for –3dB error
Tfunc_opa = tf(aol, denom);

% Gain compensation using R_BASE
Ao = ((1 + Hfe)* RSENSE) / ((1 + Hfe) * RSENSE + RBIAS + R_PI);
denom = [Hfe / (2 * pi * fT), 1];
Tfunc_bjt = tf(Ao, denom);
Loop_gc = tf(zeros(1, 1, 3, 3));
cl_gc = tf(zeros(1, 1, 3, 3));
beta = [1, 0.5, 0.1];
for i = 1 : length(beta)
   Loop_gc(:, :, 1, i) = Tfunc_opa * Tfunc_bjt * beta(i);
   cl_gc(:, :, 1, i) = feedback(Tfunc_opa * Tfunc_bjt, beta(i));
end

figure;
bode(Loop_gc(:, :, 1, 1),'r',Loop_gc(:, :, 1, 2),'g',Loop_gc(:, :, 1, 3),'b')
axes_handles = findall(gcf, 'type', 'axes');
legend(axes_handles(3), '\beta = 1', '\beta = 0.5', '\beta = 0.1', 'Location', 'Northeast');
title('Loop Gain vs. \beta')

figure;
step(0.15 * beta(1) * cl_gc(:, :, 1, 1),'r', .15 * beta(2) * cl_gc(:, :, 1, 2),'g', .15 * beta(3) *
cl_gc(:, :, 1, 3),'b')
axes_handles = findall(gcf, 'type', 'axes');
legend(axes_handles(2), '\beta = 1', '\beta = 0.5', '\beta = 0.1', 'Location', 'Northeast');
ylabel('LED String Current (A)')
title('Current regulator step response with different \beta')
```